WELCOME TO ESSCIRC 2010

GENERAL CHAIRS'S MESSAGE

On behalf of the Organizing Committees of ESSCIRC 2010, it is our pleasure to welcome you to the 36th European Solid-State Circuits Conference. ESSCIRC 2010 runs parallel to his sister conference ESSDERC 2010, covering all aspects of modern solid-state systems, circuits and devices at a single event. In combination, these two conferences provide a unique forum where technologists, device experts, and circuit and system designers can interact. This interaction is instrumental to fully exploiting the potential of modern devices and technologies when confronting the challenges of system-on-chip (SoC) integration. As a delegate at ESSCIRC-ESSDERC 2010 you will have the opportunity to learn of the latest advances in these fields, and to meet those who have dared, pioneered, and succeeded.

The conferences are to be held at the Barceló Hotel Renacimiento, on the Isla de la Cartuja, an island located between two branches of the Guadalquivir river which today is home to the Cartuja 93 technology business park. Seville's downtown (El Centro) is very close by and, from there, visitors will find Seville's major monuments and shops just a few short steps away.

This year, a total of 265 submissions from 34 different countries were received for ESSCIRC including 148 papers from Europe, 70 from Asia-Pacific, 32 from North and South America and 15 from the Middle East and Africa. This is proof of the truly international nature of ESSCIRC. The Technical Program Committee with about 110 world-class experts from academia and industry selected 114 papers for oral presentation. Twelve plenary presentations by guest speakers complete the program by focusing on highly relevant topics selected by the Technical Program Committees of both conferences. In addition to the conference programs, a pre-conference day with introductory tutorials and a post-conference day with workshops showcasing work currently being carried out by European research consortia will also be held.

We would like to thank the Steering Committee of ESSCIRC-ESSDERC for giving us the opportunity to organize this event. The meeting has been organized by members of the Institute of Microelectronics of Seville (CNM-CSIC), the University of Seville and the University of Granada. We would like to thank

GENERAL CHAIRS'S MESSAGE

the authorities of these institutions for allowing us to devote part of our time to the organization.

We have been extremely fortunate to have the help of an outstanding team of volunteers of the Organizing Committee and the Technical Program Committee, who have all worked very hard. We are hugely indebted to all these volunteers. Our warm thanks to all of them for their dedication, enthusiasm and professionalism.

Last but not least, we would like also to express our greatest appreciation to all the authors who submitted papers to the conference and to all delegates, tutorial lecturers and plenary speakers who have travelled to Seville to interact and share their thoughts during the Conference. They will play a leading role at the event.

Enjoy ESSCIRC-ESSDERC 2010 and your visit to Seville. We hope to see you all back here more often!

Welcome / Bienvenidos !!

José L. Huertas
Ángel Rodríguez-Vázquez
General Chairs - ESSCIRC-ESSDERC 2010

ABOUT IMSE/US

The “Instituto de Microelectrónica de Sevilla” (IMSE) is a R&D centre specialized on design and test of analogue, mixed-signal and sensory-processing integrated circuits as well as on their use in any application context, specially in RF, microsystems, data conversion...

IMSE, together with the Microelectronics Institutes in Barcelona (IMB) and Madrid (IMM) form the Spanish National Microelectronics Centre (CNM) operated under the umbrella of “Consejo Superior de Investigaciones Científicas” (CSIC).

The personnel from IMSE has been carrying out research, teaching and technology transfer for more than 20 years. In particular, teaching is done as regular courses offered by the University of Seville and as courses and seminars given elsewhere on demand. The PhD thesis and the research projects within IMSE are mainly focusing on the implementation of innovative concepts in silicon, paying special attention to their experimental verification.

Starting on 2009, IMSE is providing external services based on a tester Agilent 93000, giving training, technical support and test-board design for implementing and debugging test procedures both in analogue and digital.

In addition, IMSE offers an academic master: *Master in Microelectronics Design and Applications of Micro/ Nanometric Systems*. It is oriented to provide professionals with a scientific, technological, and sociol-economic education in Micro - Nano electronics.

On the other hand, the “Universidad de Sevilla” (US) is a top-ranked European university. Founded under the name of Colegio Santa María de Jesús in 1505, the university of Seville, with a student body of over 55,000, is one of the most important higher education institutions in the country.

The Faculties, Technical High Schools, Polytechnics and University Schools are the centres in charge of organizing the teaching as well as the academic, administrative and managerial processes leading to obtaining a degree.

Public service of higher education is assigned to this university and carried out through the study, teaching and research as well as through the generation, development and diffusion of knowledge at society and citizenship's service, offering as well, scientific and technical support for the cultural, social, economic and territorial development and the concern for training professionals.

About University of Granada (please see ESSDERC Programme, pages 3 and 4).

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9:50	**Joint Plenary Lecture**
10:40	**Coffee Break**
11:00	**Fringe Poster Briefing Session**
11:20	**ESSCIRC Sessions**
13:00	**Lunch**
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16:50	**Coffee Break**
17:20	**ESSCIRC Sessions**
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Thursday, September 16th, 2010

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9:00	**Joint Plenary Lecture**
9:50	**Joint Plenary Lecture**
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ESSCIRC SCHEDULE

SCHEDULE

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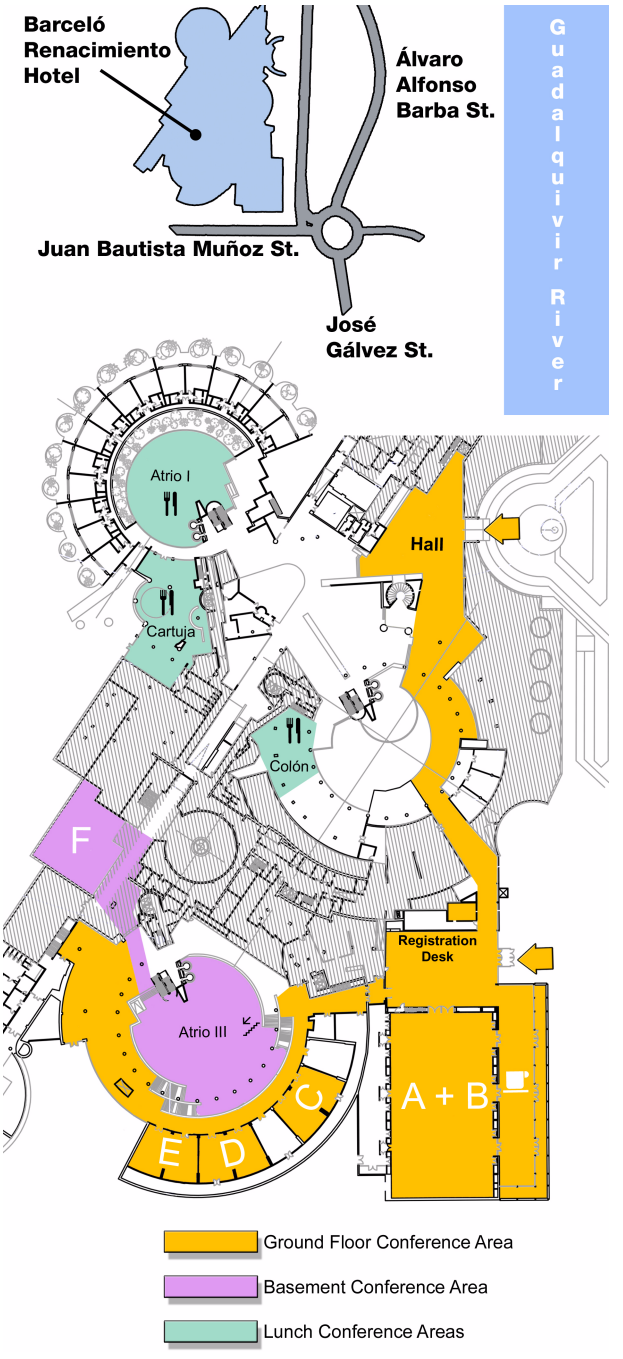
MEETING ROOMS FLOORPLAN

MEETING ROOMS FLOORPLAN



PROGRAMME AT A GLANCE

PROGRAMME AT A GLANCE

Tuesday September 14th, 2010

Time	ROOM B	ROOM E	ROOM D	ROOM A	ROOM C	ROOM F
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10:40-11:00	COFFEE BREAK					
11:00-11:20	FRINGE POSTER BRIEFING SESSION					
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14:50-15:50	A4L-B Alternative FETs	A4L-C Special characterization methods and structures	A4L-D Advances in algorithms and simulation methods	A4L-A (ROOM A) ESSCIRC PLENARY: Terahertz Imaging with CMOS/BiCMOS Process Technologies SPEAKER: Dr. Ullrich Pfeiffer (University of Wuppertal, Germany)		
15:50-16:50	A5L-A (ROOM B) ESSDERC PLENARY: GaN-on-Si Technology, A New Approach for Advanced Devices SPEAKER: Dr. Tomás Palacios (Massachusetts Institute of Technology, USA)			A5L-F Amplifiers I	A5L-G Micropower AD interfaces	A5L-H mm-Wave Transceivers
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17:20-18:40	A6L-B SOI MOSFETs	A6L-C Ferromagnetic and polycrystalline devices	A6L-E Cryptographic Processors	A6L-F SAR ADCs and DACs	A6L-G Power Management	A6L-H mm-Wave Frequency Generation
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09:50-10:40	B2L-A (ROOM A+B) JOINT PLENARY: Energy Harvesting - from Devices to Systems SPEAKER: Dr. Yiannos Manoli (IMTEK - University of Freiburg and HSG-IMIT)					
10:40-11:20	COFFEE BREAK					
11:20-13:00	B3L-B Simulation of advanced silicon devices	B3L-C Photodetectors	B3L-D Silicon and Gallium Nitride power devices	B3L-F TDCs and Timing Circuits	B3L-G Sensors	B3L-H Power Amplifiers
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14:50-15:50	B4L-B Modeling of temperature and stress impacts	B4L-C Advanced FET characterization	B4L-D Phase Change Memories	B4L-A (ROOM A) ESSCIRC PLENARY: Analog Mixed-Signal Circuits in Advanced Nano-scale CMOS Technology SPEAKER: Dr. Ian Young (Intel Corporation)		
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Thursday September 16th, 2010

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15:50-16:50	C5L-A (ROOM B) ESSDERC PLENARY: Trends & Perspectives for Electrical Characterization & Reliability Assessment SPEAKER: Dr. Guido Groeseneken (IMEC)		C5L-E Emerging Memories	C5L-F mm-wave radar and imaging		C5L-H UWB Communications
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17:20-18:40	C6L-B Analytical/compact models	C6L-C Electromechanical Devices	C6L-E Circuit Design in Emerging Technologies	C6L-F Signal Processing Platforms		C6L-H Optical Communications

PROGRAMME AT A GLANCE

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WELCOME TO SEVILLA

Seville, rich millenary heiress of different cultures that settled along the shores of the Guadalquivir River, preserves and pampers its world famous monumental architecture. At the same time it proudly and brilliantly treasures mysterious secrets that romantic authors attempted to release in mythical works such as Carmen, The Barber of Seville or Don Juan, amongst many others.

Nonetheless, the Seville that we wish to introduce to you today is a synopsis of the values of its past heritage and modernity of its present reality. Such a symbiosis holds the city's historical character which offers contemporary infrastructures which convert the city into a first class tourist destination, not just for the individual tourist but also for the business person attending conferences or incentive trips.

THE CATHEDRAL AND THE GIRALDA

"Let us create such a building that future generations will take us for lunatics". That's what churches authorities repudetly agreed back in 1401. And they certainly got themselves the big and magnificent Cathedral, one of the largest catholic churches in the world: the main building is 126m long and 83m wide. The original mosque's beautiful minaret (for the cathedral was built over the main mosque that fell to the christians in 1248), La Giralda, still stands on its eastern side, but the cathedral's bulky exterior gives few other hints of the treasures within.

Price per person: 8€ (general ticket)
Hours: Mon-Sat: 11am - 5pm. Sun: 4.30pm - 6pm
Phone: (+34) 95 421 49 71

ALCÁZAR

Residence of many generations of kings and caliphs, the not-to-be-missed Alcázar is an intriguing, beautiful complex of gardens, patios, and royal rooms, and it is intimately associated with the lives and loves of many Muslim and Christian rulers, above all Pedro I of Castilla, who was known as Pedro

El Cruel and Pedro El Justiciero (the Cruel and the Justice-dispenser) depending which side of him you were on.
Price per person: 7,5 € (general ticket)
Hours: Mon-Sun: 9.30am - 7pm
Phone: (+34) 95 450 23 23

SANTA CRUZ, THE CENTRO AND THE ARENAL

Santa Cruz is Seville's medieval Judería (Jewish quarter), today a tangle of quaint, winding streets and lovely plant-decked plazas perfumed with orange blossom. Plaza de Santa Cruz, Plaza Doña Elvira, the 17th-century Hospital de los Venerables Sacerdotes, are spots the visitor won't want to miss here. The real centre of Sevilla, El Centro, is densely packed with narrow streets and broken up by squares and streets (Calle Sierpes, Casa Pilatos, Plaza del Salvador,...) around which the city's life has revolved for aeons. The Arenal, a short walk from the Cathedral, brings the visitor to the Río Guadalquivir. Seville's most interesting sights here include the Torre del Oro (a 13th-century islamic watch tower), Plaza de Toros (the bullring, one of the most handsome in Spain and probably the oldest), the Hospital de la Caridad and the Museo de Bellas Artes (Fine-Arts Museum), which is the second Art Gallery in the country.

CLIMATE

Seville has a Mediterranean weather due to the oceanic influences nearby. In the winter the temperatures are mild, and in the summer the weather is hot. Precipitation varies along the year, concentrated in the period October to April. December is the wettest month, and the coldest are January and February. June, July and August are the hottest months. The weather in Seville in September is usually warm. It is sunny almost every day. First rains are late September or

WELCOME TO SEVILLA

early October and rarely last more than a day or two. In that season of the year, the days are long: the sun rises around 8.00am, and sets around 8.30 pm.

FAST FACTS

Country: Spain / España
Status: city / capital of Andalusia
Population: 720,000 in the city + another 400,000 in its outskirts
Language: Spanish
Time zone: UTC+2 at summer time (March 28 to October 31), UTC+1 at winter time (From October 31)
Country dialling code: +34
Telephone area code for Seville: 95
Currency: Euro is the official currency of Spain. Euro (€) = 100 cents. Notes are in denominations of €500, 200, 100, 50, 20, 10 and 5. Coins are in denominations of €2, 1 and 50, 20, 10, 5, 2 and 1 cents. Money can be taken from cash machines (ATMs) which accept most international cards.
Health and security:
Emergency service (Fireman, police, civil protection, sanitary emergency) phone number: 112
National police: emergency telephone number: 091
Local police: emergency telephone number: 062
Medical emergencies: emergency telephone number: 061
Tipping: tipping in Spain is not obligatory but it is common to leave some change or to give a tip of 5–10%. There are no added service charges on the final bill at any hotel restaurant, or bar...
Electricity: 220 volts, 50 Hz - round two-pin plugs are used
Measures: Weight measured in kilograms, distances measured by the metric system, temperature measured in degrees Celsius
Tourist Office: Paseo de las Delicias, 9 (Costurero de la Reina) 41012 Sevilla. Phone: +34 95 423 44 65
Seville tourism information can be found at **www.turismosevilla.org** and **www.andalucia.org**

PHARMACIES

A chemist's or drugstore is known as a Farmacia and they can be identified by a large green or red cross sign outside. They tend to keep the same working hours as other shops and if closed, usually display a sign indicating the nearest pharmacy that is open. As well as selling prescription medicines, they also offer free advice about minor injuries or ailments and they will happily suggest non-prescription treatments. Usually open from 9.30am to 1.30pm, and from 4.30am to 8.00pm. Besides you can find pharmacies that

open 24 hours. Pharmacies follow a rolling late-hour schedule, which is published in the newspapers and the internet, and is posted at all pharmacies.

HOURS OF BUSINESS/SHOPS IN SEVILLE

Most offices in Seville open at 9.00 am and many close for a couple of hours in the afternoon, although this varies with companies. The most common business time-table is from Monday to Friday, from 9.30am to 1.30pm, and from 5.00pm to 8.00pm. Many shops also open on Saturdays from 9.30am to 1.30pm. Big shopping centres and department stores open from 10.00am to 9.00pm or 10.00pm uninterruptedly, except Sundays and local holidays.

BANKS OPENING TIMES:

Banks are generally open Monday-Friday from 8.30am to 2.00pm, and sometimes on Saturday from 8.30am to 1.00pm.

CURRENCY EXCHANGE

There are many places to exchange currency, the banks being the ones with best rates. There are also foreign exchange outlets in the airports and even in some hotels and restaurants, although the rates are usually not so favourable. Withdrawing money at a cash point (ATM) is often the most convenient and economic way to obtain Euros and there are ATMs all over the city. Many are located inside banks or in their facades.

CREDIT CARDS, TRAVELLERS CHEQUES

Credit cards are widely accepted at establishments throughout Seville and these include Visa, EuroCard, Access, MasterCard and American Express. In some stores, you may be asked to enter your PIN (Personal Identification Number) into a keypad for security purposes. Some shops do not accept credit card payment for a small monetary amount. Travellers cheques, accompanied by a passport, are also accepted in most hotels, restaurants and shops.

ATMS (AUTOMATIC BANKING MACHINE)

There are ATMs almost everywhere, and most support Visa/Plus, Cirrus, and other popular systems. Just look for the signs next to the ATM or on the display itself. ATMs are easy to use here and all offer English as well as other languages.

IVA (VAT) REFUND

How to get IVA (VAT) back on shopping: If a buyer's residence is outside the European Union, then he/she can claim back the tax on purchases, as long as they amount for more than 90.15 Euro in each establishment. In order to do so, you

WELCOME TO SEVILLA

should ask for a tax-free receipt, wherever you see the Spain Refund Tax-free Shopping logo, at the point of sale. The Tax-Free cheque must be stamped, always before the check-in. Show the goods to customs when leaving the country. You can claim your money in the SPAIN REFUND cash agents in airports and borders. (Tax free Spain refund information www.spainrefund.com, www.globalrefund.com)

CURRENCY CHOICE LOGO

The Currency Choice logo next to a credit card terminal means that there you can pay by credit card in your own national currency. The amount on the receipt is the sum that will be debited to your bank. No hidden fees, no surprises when you get back home.

VISA INFORMATION

Anyone wishing to travel to and enter Spain must have a valid passport and/or the appropriate Spanish Visa. We recommend contacting your local Spanish consulate or Embassy for more information on these requirements.

For further information about Sevilla, please check **www.infosevilla.com**

CONFERENCE VENUE

The conferences, tutorials and workshops will be held at the:

BARCELÓ RENACIMIENTO HOTEL

Isla de la Cartuja, s/n E-41092

The avant-garde Barceló Renacimiento***** is a modern, top-quality hotel located in Seville, on the Island of La Cartuja, on the banks of the Guadalquivir river, that is today home to the Cartuja scientific and technologic park. It is the best equipped hotel in the city to accommodate groups, conferences, congresses and incentive trips, boasting its own 25-room Convention Center.

Conveniently located, just a few minutes away from Seville's historic center, the high-speed AVE train station and the airport close by, is an attractive option for both business travelers and people interested in urban sight-seeing.

Barceló Renacimiento's facilities include 25 meeting rooms and 2 atriums for events. The Convention Center Gran Sevilla was opened in 2002 and it provides fully equipped 1,024m2 ideal for any kind of event. It can be turned into 3 independent rooms where natural light is very important. Besides, there is an exhibition area of 800m2.

Barceló Renacimiento hotel is member of the International Congress and Conventions Association (ICCA).

LOCATION

COORDINATES:
LAT: 37º 24´ 35´´ N
LONG: -5º 59´ 43´´ W - E
Distance to the city centre: 1-2 kilometres.
Distance to the airport: 10 kilometres.
Train station: 20 minutes.
Near by City bus lines C1 and C2.

CONFERENCE VENUE

A range of hotels (see map below) to suit all budgets and requirements are also within a short distance of the meeting venue.

How to reach the venue

By City Bus

There is a good city bus service from/to the conference site to/from the city center (it takes around 10-20 minutes). Walking distance to bus stop: 3-5 minutes.

Please, see below section "Getting around" for further information.

BY TAXI

Please, see section below on "Getting around" for further information.

RAILROAD/RAILWAY

The railroad transportation system connects all major urban centers. The **Santa Justa train station** serves as an important hub for connections between the Andalusia´s main cities and all of the autonomous regions of Spain and Europe.
AVEs (high speed trains) connect to/from Cordoba (around 30€ to 50€, 40 minutes), Malaga (36€, 2 hours), Madrid (usually 64€ to 70€, 2½ hours) or Barcelona (80€ to 250€ 5½ hours).
In addition to the AVE service, this modern station concentrates all railway traffic, with trains to various towns of the province, to all the capitals of Andalusia and to other Spanish cities such as Barcelona, Valencia, Alicante and Cáceres.
The **Santa Justa Train Station** is located at Avda. Kansas City s/n. 41007 Sevilla, Information phone +34 902 320 320. International information phone: +34 902 243 402
For further information about train services and other train types and destinations please visit the website at www.renfe.es

ROADS

Highway and access roads and rapid beltways provide precise connections to all neuralgic points of the city and its surroundings. Seville has now become one of Spain's best connected cities by road, with highways connecting all Andalusia´s main cities as well as Madrid and Portugal. Main access roads are the A-92, N-IV, A-4, and A-49.

GETTING AROUND

City Buses:

(Spanish name: *autobús*) Buses are the cheapest way to get around Sevilla. A single bus ride is 1.20€, but you can buy a voucher with 10 trips (*bonobus*) from 7€ at a newsstand or tobacco shop. The city bus network is based around four lines- C-1, C-2, C-3, and C-4- which follow circular routes, linking the main transport terminals and the city centre. Four transversal lines and a series of radial lines which lead into the centre from the four points of the compass complete the bus network.
You can pick up a bus route map, *the Guía del Transporte Urbano de Sevilla*, from tourist offices or from information booths at major stops (including Plaza Nueva, Plaza de la Encarnación and Avenida de Carlos V).
Information Phone: 010 (press 5) Web Site: www.tussam.es

On the other hand, Seville has two bus stations, each providing services to separate cities:·

-Prado de San Sebastián, just southeast of the Barrio de Santa Cruz, provides bus services to cities of Andalusia. Address: Manuel Vázquez Sagastizábal s/n. - Sevilla. Phone: +34 95 441 71 11

-Plaza de Armas, by the Cachorro's bridge, connects with the rest of Spain, the Province of Huelva, and Portugal. Address: Avenida del Cristo de la Expiración, s/n. - Sevilla. Phone: +34 95 490 80 40

Sightseeing tour buses:

Tour buses can be a great way to get around Seville. You have the option of traveling the full circuit and getting an overview of what to expect in the city or get on and off as many times as you want, seeing the sights as you go.

Web site: www.busturistico.com

Taxis:

Taxi stops are located on several central streets and squares. However, taxi can be hailed any place in the city when they show the *libre* (free) sign or a green light.

Many of the short cab rides cost between 3-6€. From the airport to the city center or the opposite there is now a flat rate. The fee is 17€ during the day and 20€ during holidays, Sundays or night (after 10pm).

Phones: +34 95 467 55 55 / +34 95 458 00 00 / +34 95 462 22 22

Web sites: www.taxisevilla.es, www.taxigiralda.es

Subway and tram:

(Spanish name: *metro*) Seville's subway system has only one line that goes from the west to the south part of the city and surrounding suburbs. A single ride is 1.30€.

(Spanish name: *tranvía metro centro*) (T1) is a surface tram by the center of Seville that connects Plaza Nueva to Prado de San Sebastián bus station, with a total of 1.3km. This route covers the pedestrian area in the city center.

Web site: www.metrodesevilla.org

Bicycle:

(Spanish name: *bicicleta*) Sevici is the name of a community bicycle program in Seville. Its purpose is to cover the small and medium daily routes within the city in a climate friendly way. More than 250 stations and 2500 bikes will be available. The stations are situated throughout the inner-city with a distance of around 200 metres between each one, with many situated next to public transport stops to allow for intermodal use. The bikes can be borrowed from, and returned to, any station in the system, making it suitable for one way

travel. Each station has between 10 and 40 parking slots to fix and lock the bicycle.
There is a short term subscription for tourists with an unlimited number of journeys during 7 consecutive days (a deposit of 150€ is mandatory).
Web site: www.sevici.es

Other ways:

On foot: The city center of Seville is not very large and it is easy to walk to all the tourist spots, a lot of fun to walk around. The centre has almost become completely car-free.

Horse-Drawn carriage tour: it is very typical way to get around Seville. You have the opportunity to get more information and register for this tour at a reduced price for ESSCIRC/ESSDERC attendees at: http://www.esscirc2010.org/registro/excursiones/registration_form.php

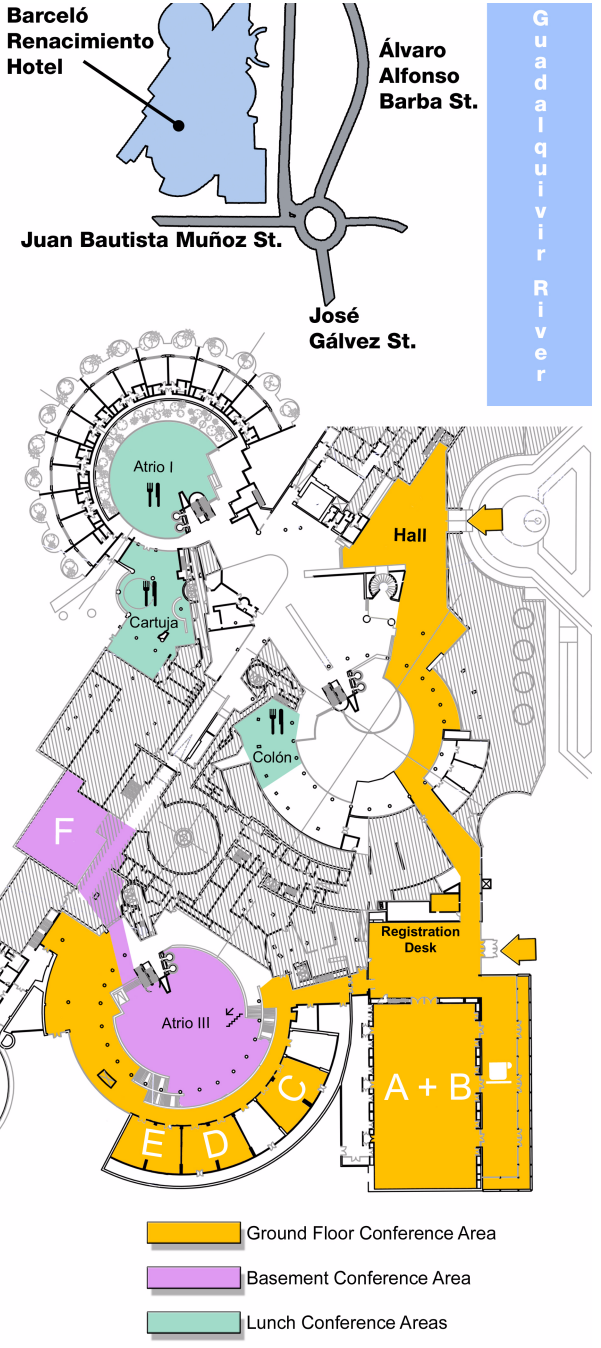
River cruises along the Guadalquivir River: the emblematic Andalusian river, the Guadalquivir is the only navigable river in Spain. You have the opportunity to get more information and register for this cruise at a reduced price for ESSCIRC/ESSDERC attendees at: http://www.esscirc2010.org/registro/excursiones/registration_form.php

Sevilla Tourist Card

Sevilla Card, the Seville tourist card, will help you discover the city and enjoy your stay and save money. Its price is from 29€ to 50€ per day. Some advantages with the card are:
-Free admission to most museums and monuments in the city and environs.
-Unlimited use of sightseeing buses.
-Boat rides on the Guadalquivir River.
-*Isla Mágica* Theme Park.
-Besides you will be able to enjoy discounts in shops, restaurants, shows and leisure centres for adults and children.
-Guide/map with information about museums, services included and participating establishments.
-A free "traditional tapa" as well as a drink.
Web site: www.sevillacard.es

CONFERENCE VENUE

CONFERENCE VENUE



CONFERENCE INFORMATION

LANGUAGE

The official language of the Conference is English.

WEBPAGES

ESSCIRC 2010 webpage: **www.esscirc2010.org**
ESSDERC 2010 webpage: **www.essderc2010.org**

NAME BADGES

All participants and accompanying persons are asked to wear their name badges in a visible place. Entrance to sessions is restricted to registered delegates only. Entrance to meeting halls, poster and exhibition areas is granted to badge holders.

SPEAKERS BRIEFING

Authors should meet their chairperson in the session room 15 minutes ahead the respective sessions.

INTERNET ACCESS

Wireless internet access will be available at the conference venue without charge.

CONFERENCE PROCEEDINGS

All participants will receive a copy of either the ESSDERC or the ESSCIRC Proceedings and a CD containing the accepted papers for both.

BEST PAPER AWARD

Papers presented at the conferences will be considered for the Best Paper Award and for the best “Young Scientist“ Paper Award. The selection will be based on the results of the paper selection process and the judgment of the conference participants. The award delivery will take place at ESSCIRC/ESSDERC 2011.

INSURANCE DISCLAIMER

Participants are responsible for their own insurance. The organizers cannot take responsibility for any accident, loss or damage to participants or their property during the event.

COMPLAINTS

While we hope that your time at the conference is enjoyable, if you encounter a problem during your stay, please report it to the registration desk as soon as possible. The conference team will make every effort to rectify the issue.

CONFERENCE OVERVIEW

In addition to contributed papers and plenary lectures, the event will include tutorials, exhibits and satellite workshops to be organized before and after the conference.
An attractive social program will complement the event, featuring a welcome reception, a gala dinner with awards ceremony, and excursions.

SCHEDULE AT A GLANCE

MONDAY, SEPTEMBER 13TH, 2010
Tutorials

TUESDAY, SEPTEMBER 14TH, 2010
Conference Opening
Technical Sessions
Welcome Reception

WEDNESDAY, SEPTEMBER 15TH, 2010
Technical Sessions
Gala Dinner

THURSDAY, SEPTEMBER 16TH, 2010
Technical Sessions

FRIDAY, SEPTEMBER 17TH, 2010
Workshops

THE AIM OF THE CONFERENCE

The aim of the ESSCIRC conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state circuits.

GENERAL SCOPE OF THE CONFERENCE

ESSCIRC and its sister conference ESSDERC, which deals with solid-state devices and technologies, are governed by a single Steering Committee. The increasing level of integration for system-on-chip (SoC) design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers.
While keeping separate Technical Program Committees, ESSCIRC and ESSDERC will share Plenary Keynote Presentations bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

THEMES OF THE CONFERENCE

The conference's core themes are set out below. The programme committee also welcomes novel contributions from other related areas.

ANALOGUE CIRCUITS

Amplification stages, Power amplifiers for audio applications, Continuous- and discrete-time filters, Switched-capacitor circuits, Comparators, Nonlinear circuits, Voltage/current references, HV circuits.

DATA CONVERTERS

Nyquist rate converters, Oversampled A/D and D/A converters, Sample-and-hold circuits, A/D and D/A converter calibration and error correction circuits, Adaptive and smart data converters.

RF AND MM WAVE

RF/IF/analog baseband circuits, LNAs, Mixers, Power amplifiers, IF amplifiers, Power detectors, Modulators-Demodulators, VCOs, PLLs, Frequency synthesizers, Frequency dividers, Integrated passive components.

WIRELESS AND WIRELINE COMMUNICATION CIRCUITS AND SYSTEMS

Receivers/transmitters/transceivers for wireless systems, Base stations and handsets, Advanced modulation systems, TV/radio/satellite receivers, Radar.

SENSORS, IMAGERS AND MEMS

Sensor subsystems and interfaces, Accelerometers, Temperature sensing, Imaging and smart imaging chips, Vision systems on chip, AMOLED, MEMs subsystems, RF MEMs.

DIGITAL CIRCUITS

Digital circuit techniques, I/O and inter-chip communication, Reconfigurable digital circuits, Clocking, Arithmetic building blocks.

PROCESSORS, MEMORIES AND INTERFACES

Memories, Microprocessors, DSPs, Gigabit serial links, Clock data recovery, Equalization, Memory interfacing, Bus interfacing, Multi-rate link IC ´s.

BIO-MEDICAL AND BIO-ELECTRONIC CIRCUITS & SYSTEMS

Implantable electronic ICs, Bio-electronic integrated systems, Bio-medical imagers, Bio-MEMS integrated systems, Lab-on-chip, Wireless body area networks.

CIRCUIT & SYSTEMS IN EMERGING TECHNOLOGIES

Digital, analogue and mixed-signal circuits using emerging devices such as: Multi-gate MOS- FETs (Double-Gate MOS-

FETs, FinFETs, Triple-Gate MOSFETs); Flexible electronic components; Organic transistors; Nanowires/nanotubes; Quantum devices.

POWER MANAGEMENT AND ENERGY SCAVENGING

Energy transducers, Power regulators, DC-DC converters, LDOs, Boost converters, Buck converters, LED drivers, Sequencers and supervisors, Green circuits.

MEALS AND REFRESHMENTS

All meals and refreshments will be served at scheduled times during the conference programme.

MONDAY, SEPTEMBER 13TH, 2010.

Morning refreshments	In front of Rooms A+B
Lunch	Colón, Cartuja, Atrio I
Afternoon refreshments	In front of Rooms A+B

TUESDAY, SEPTEMBER 14TH, 2010

Morning refreshments	In front of Rooms A+B
Lunch	Colón, Cartuja, Atrio I
Afternoon refreshments	In front of Rooms A+B
Welcome Reception	place to be announced

WEDNESDAY, SEPTEMBER 15TH, 2010

Morning refreshments	In front of Rooms A+B
Lunch	Colón, Cartuja, Atrio I
Afternoon refreshments	In front of Rooms A+B
Gala Dinner*	Convention Centre Sevilla

THURSDAY, SEPTEMBER 16TH, 2010

Morning refreshments	In front of Rooms A+B
Lunch	Colón, Cartuja, Atrio I
Afternoon refreshments	In front of Rooms A+B

*The Gala dinner is included in the registration conference fee. To buy additional tickets, please contact to the registration desk.

Participants with special dietary requirements who have not previously informed about it please contact to the registration desk in order to provide an alternative menu.

SOCIAL PROGRAMME

TUESDAY, SEPTEMBER 14TH, 2010

WELCOME COCKTAIL

A Welcome reception for ESSDERC-ESSCIRC will be offered. For further details, please visit the conference webpage.

WEDNESDAY, SEPTEMBER 15TH, 2010

GALA DINNER

A Gala Dinner for ESSDERC-ESSCIRC will be held at 'Centro de Convenciones y Congresos Sevilla' (Convention Centre Sevilla).

The new Convention Centre Sevilla offers adequate spaces for many different events, spacious reception areas and gardens where enjoy traditional Spanish food and live entertainment.

Only 15 minutes away from the city of Seville (coaches will be provided to transport participants).

Bus departure at 21:00 from the Barceló Renacimiento Hotel.

To know more about the Centro de Convenciones y Congresos Sevilla, please visit the website at www.centrosevillacongresos.com

OPTIONAL LEISURE ACTIVITIES

SIGHTSEEING TOURS AND ACTIVITIES

You have the opportunity to make different sightseeing tours and activities offered at a reduced price for ESSCIRC / ESSDERC attendees and accompanying persons.
To register and get more information, please visit http://www.esscirc2010.org/registro/excursiones/registration_form.php

ACTIVITIES (13 - 19 SEPTEMBER 2010)

Historic Sevilla
Departure Days: Wednesday, Friday, Sunday
Duration: 3.5 hours
Departure Point: Hotel or place assigned by the agency
33€ Tax Included

Classic Seville - Morning Tour
Departure Days: Monday, Tuesday, Thursday, Saturday
Duration: 3.5 hours
Departure Point: Hotel or place assigned by the agency
33€ Tax Included

Artistic Sevilla - Afternoon Tour
Departure Days: Monday, Wednesday, Friday, Sunday
Duration: 3 hours
Departure Point: Hotel or place assigned by the agency
29€ Tax Included

Monumental Sevilla - Morning Tour
Departure Days: Monday, Tuesday, Thursday, Saturday
Duration: 3 hours
Departure Point: Main door of the Starbucks cafe - San Fernando Street 1 (Puerta Jerez)
19€ Tax Included

Typical Sevilla
Departure Days: Wednesday, Friday, Sunday
Duration: 3,5 hours
Departure Point: Main door of the Starbucks cafe - San Fernando Street 1 (Puerta Jerez)
25€ Tax Included

Roman City of Itálica - Afternoon tour
Departure Days: Tuesday, Thursday, Saturday
Duration: 4 hours
Departure Point: Hotel or place assigned by the agency
25€ Tax Included

Sevilla Night
Departure Days: DAILY

OPTIONAL LEISURE ACTIVITIES

Duration: 3 hours
Departure Point: Hotel or place assigned by the agency
45€ Tax Included

Granada

Departure Days: Wednesday, Friday, Sunday
Duration: 12 hours
Departure Point: Hotel or place assigned by the agency
110€ Tax Included

Cordoba

Departure Days: Tuesday, Thursday, Saturday
Duration: 9 hours
Departure Point: Hotel or place assigned by the agency
85€ Tax Included

Jerez & Cádiz

Departure Days: Tuesday, Thursday
Duration: 9 hours
Departure Point: Hotel or place assigned by the agency
94€ Tax Included

Tickets River Cruise along the Guadalquivir

Departure Days: DAILY
Duration: 1 hours
Departure Point: Paseo Alcalde Marqués de Contadero (Muelle Torre del Oro)
12€ Tax Included

Tickets River Cruise + Flamenco Show (AFTERNOON)

Departure Days: DAILY
Duration: 3 hours
Departure Point: Boat: Muelle Torre del Oro / Flamenco: María Auxiliadora Avenue 18 B
39€ Tax Included

Tickets River Cruise + Flamenco Show (NIGHT)

Departure Days: DAILY
Duration: 3 hours
Departure Point: Boat: Muelle Torre del Oro / Flamenco: María Auxiliadora Avenue 18 B
39€ Tax Included

Hop On Hop Off Tour Bus

Departure Days: DAILY
Duration: 24 hours
Departure Point: Torre del Oro
14€ Tax Included

OPTIONAL LEISURE ACTIVITIES

Sevilla Walking Tour + River Cruise
Departure Days: DAILY
Duration: 2.5 hours
Departure Point: Torre del Oro
28€ Tax Included

Walking Tour + Horse-Drawn carriage tour
Departure Days: DAILY
Duration: 2.5 hours
Departure Point: Plaza de España
48€ Tax Included

Romantic Sevilla
Departure Days: DAILY
Duration: 2 hours
Departure Point: Plaza de España
75€ Tax Included

MUSEUMS IN SEVILLE

Free entry for EU citizens. Non-EU citizens: 1,50 € to the following museums:
-Museo arqueológico de Sevilla (**Archaeological Museum**)
http://www.museosdeandalucia.es/cultura/museos/MASE/?lng=en
-Museo de Bellas Artes (**Museum of Fine Arts**)
http://www.museosdeandalucia.es/cultura/museos/MBASE/?lng=en
-Museo de artes y costumbres populares (**Museum of Arts and Traditions**)
http://www.museosdeandalucia.es/cultura/museos/MACSE/
-Conjunto arqueológico Itálica (**Archaeological Ensemble Italica**)
http://www.museosdeandalucia.es/cultura/museos/CAI/
-Conjunto arqueológico de Carmona (**Archaeological Ensemble Carmona**)
http://www.museosdeandalucia.es/cultura/museos/CAC/?lng=en
Non-free entry:
-Monasterio de la Cartuja (**Cartuja Monastery)** and Centro andaluz de arte contemporáneo (**Andalusia Contemporary Art Centre**)
http://www.juntadeandalucia.es/cultura/caac/english/frame.htm
1,80€ Visit the monument or to the temporary exhibitions
3,01€ Complete visit

HIGH PERFORMANCE MIXED SIGNAL: BUSINESS AND TECHNOLOGY

Dr. René Penning de Vries, NXP Semiconductors

René Penning de Vries, NXP Semiconductors, Netherlands
Hans Rijns. NXP Semiconductors, Netherlands
Maarten Vertregt. NXP Semiconductors, Netherlands

Abstract
The increasing sophistication of technical solutions provided by the semiconductor industry, will more and more be enabled by ICs that bridge the analog outside world with transceivers, power management, and sensor and actuation functions to the digital world of signal processing and storage. Many of these application optimized functions will emerge in the coming years and will find differentiation by mixed-signal designs in specific –More-than-Moore-- technologies. We believe this class of circuits provides great new growth opportunities to the semiconductor industry.

Dr. René Penning de Vries is Senior Vice President and Chief Technology Officer of NXP Semiconductors BV.
René is responsible for the product creation processes at NXP, focusing on the key areas of Innovation, Technology and Research.
René previously held the position of CTO at Philips Semiconductors prior to the formation of NXP in 2006. He started working for Philips Research in 1984. His career evolved from various technical and managerial roles in CMOS development, into management of platform and design technology as well IP creation. Later, system technology and research were added to his portfolio.
During his career, René worked and lived in the US, France and in Singapore, where he was VP of Technology in SSMC.

3D INTEGRATION TECHNOLOGY: STATUS AND APPLICATION DEVELOPMENT

Dr. Peter Ramm, Fraunhofer IZM Munich Division

Peter Ramm, Fraunhofer IZM Munich Division, Germany
Armin Klumpp, Fraunhofer IZM Munich Division, Germany
Josef Weber, Fraunhofer IZM Munich Division, Germany
Nicolas Lietaer, SINTEF ICT, Norway
Maaike Taklo, SINTEF ICT, Norway
Walter De Raedt, IMEC-SSET, Belgium

Thomas Fritzsch. Fraunhofer IZM. Germany
Pascal Couderc. 3D-PLUS, France

Abstract
As predicted by the ITRS roadmap, semiconductor industry development dominated by shrinking transistor gate dimensions alone will not be able to overcome the performance and cost problems of future IC fabrication. Today 3D integration based on through silicon vias (TSV) is a wellaccepted approach to overcome the performance bottleneck and simultaneously shrink the form factor. Several full 3D process flows have been demonstrated, however there are still no microelectronic products based on 3D TSV technologies in the market - except CMOS image sensors. 3D chip stacking of memory and logic devices without TSVs is already widely introduced in the market. Applying TSV technology for memory on logic will increase the performance of these advanced products and simultaneously shrink the form factor. In addition to the enabling of further improvement of transistor integration densities, 3D integration is a key technology for integration of heterogeneous technologies. Miniaturized MEMS/IC products represent a typical example for such heterogeneous systems demanding for smart system integration rather than extremely high transistor integration densities. The European 3D technology platform that has been established within the EC funded e-CUBES project is focusing on the requirements coming from heterogeneous systems. The selected 3D integration technologies are optimized concerning the availability of devices (packaged dies, bare dies or wafers) and the requirements of performance and form factor. There are specific technology requirements for the integration of MEMS/NEMS devices which differ from 3D integrated ICs (3D-IC). While 3D-ICs typically show a need for high interconnect densities and conductivities, TSV technologies for the integration of MEMS to ICs may result in lower electrical performance but have to fulfill other requirements, e. g. mechanical stability issues. 3D integration of multiple MEMS/IC stacks was successfully demonstrated for the fabrication of miniaturized sensor systems (e-CUBES), as for automotive, health & fitness and aeronautic applications.

Dr. Peter Ramm is head of the Silicon Technology and Vertical System Integration department of Fraunhofer EMFT (formerly IZM-M) in Munich, Germany, where he is responsible for process integration of innovative devices and heterogeneous systems with a specific focus on 3D integration tech-

nologies. Peter Ramm received the physics and Dr. Rer. Nat. degrees from the University of Regensburg and subsequently worked for Siemens in the DRAM facility where he was responsible for the process integration. In 1988 he joined Fraunhofer IFT in Munich, focusing since more than two decades on 3D integration technologies. He is author or co-author of more than 100 publications, including three book chapters and 23 patents. Peter Ramm is co-editor of four peer reviewed proceedings books (Materials Research Society and Electrochemical Society) and of Wiley´s "Handbook of 3D Integration". He received the "William D. Ashman Achievement Award 2009" from the International Microelectronics and Packaging Society (IMAPS) "for pioneering work on 3D IC stacking and integration".

ENGINEERING HOPE WITH BIOMIMETIC MICRO-ELECTRONIC SYSTEMS

Dr. Wentai Liu, University of California Santa Cruz (UCSC)

Wentai Liu. University of California Santa Cruz, United States
Zhi Yang. University of California Santa Cruz, United States
National University of Singapore

Abstract

This paper focuses on biomimetic systems for building advanced neuroscience and neuroprosthetics platform with closed-loop control mechanisms. Works on neural implants consist of four major functional blocks of stimulation, recording, processing, and wireless communication, each of which has different challenges to be overcome. On-chip integration of these fundamental blocks with low power requirements inevitably needs multi-voltage and multi-signal design techniques. Combining these techniques with the stated-of-art high voltage process, high compliance voltage for miniaturized nerve/neuromuscular stimulators can be achieved. An understanding of the noise sources and their contributions within neural interface provides a better way to optimize the performance of the recording function.

On chip signal processing techniques for noise reduction, feature extraction, and data classification facilitates decision-making and closed-loop execution. Power and data telemetry links enable implanted electronic to operate wirelessly, avoiding large size battery or percutaneous physical links that are prone to damage.

Dr. Wentai Liu received BS from National Chiao-Tung University (Taiwan), MS from National Taiwan University, and PhD from the University of Michigan. In 1983, he joined North Carolina State University, where he held the Alcoa Chair Professorship in ECE and was the founder of the Analog/Mixed-Mode Design Consortium. Since 2003, he has been a professor at the University of California, Santa Cruz, where he is also the Campus Director and Thrust Leader of the NSF Engineering Research Center on Biomimetic Microelectronic Systems. His research interests include neuro-engineering, neural prosthesis, brain-machine interface, bioelectronics, transceiver, sensors and actuators, timing/clock optimization, vision/image processing. He has been working on the neural implants dealing with nerves and muscles for retina, epilepsy, muscle, eyelids, spinal cord, and bladder. Since its inception, he has been leading the engineering efforts of the retinal prosthesis to restore vision, finally leading to successful implant trials in blind patients. He has published more than 300 technical papers and two books. He received RD-100 Award, two IEEE Outstanding Paper Awards, Alcoa Foundation's Distinguished Engineering Research Award, NASA Group Achievement Award, and Outstanding Alumni Award from National Chiao-Tung University, where he also holds a Chair Professorship as the Founder and Honorary Director of Biomimetic Systems Research Center. He has served as Associate Editor for IEEE Trans. on Biomedical Engineering, Guest Editor for both IEEE Proceedings Special Issue of Biomimetic Systems and IEEE-MTT Special Issue of Wireless IC for Biomedical Applications. He is the founder of the International Conference on Neuroprosthetic Devices, which has been held twice in 2009 and 2010.

ENERGY HARVESTING - FROM DEVICES TO SYSTEMS

Dr. Yiannos Manoli, IMTEK -University of Freiburg and HSG-IMIT

Abstract

Energy harvesting micro-generators provide alternative sources of energy for many technical and personal applications. Since the power delivered by such miniaturized devices is limited they need to be optimized and adapted to the application. The associated electronics not only has to operate at very low voltages and use little power it also needs to be adaptive to the fluctuating harvesting condi-

tions. A joint development and optimization of transducer and electronics is essential for improved efficiency.

Dr. Yiannos Manoli holds the Fritz Huettinger Chair of Microelectronics at the Department of Microsystems Engineering (IMTEK), University of Freiburg, Germany. He additionally serves as director of the applied research "Institute of Micromachining and Information Technology" of the "Hahn-Schickard Gesellschaft" (HSG-IMIT).

His research interests are the design of low-voltage and low-power mixed-signal systems with over 300 papers published in these areas. The emphasis lies in Analog-to-Digital converters as well as in energy harvesting and sensor read-out CMOS circuits. Additional research activities concentrate on motion and vibration energy transducers and on inertial sensors.

Prof. Manoli received the Best Teaching Award of the Technical Faculty and Best Paper Awards from ESSCIRC 1988, PowerMEMS 2006, MWSCAS 2007 and MSE 2007. Spicy VOLTsim, a web-based animation and visualization of analog circuits, received the Multi-Media-Award of the University of Freiburg in 2005 (www.imtek.de/svs).

He holds a B.A. degree (summa cum laude) in Physics and Mathematics, a M.S. degree in Electrical Engineering and Computer Science from the University of California, Berkeley and the Dr.-Ing. Degree in Electrical Engineering from the Gerhard Mercator University in Duisburg, Germany.

TECHNICAL AND ECONOMICAL TRENDS IN WIRELESS APPLICATIONS

Dr. Martin Zander, ST Ericsson

Abstract

This paper examines technical and economical trends in wireless applications and its impact on the mobile phone industry by analyzing different historical phases that the industry gone through since the early 1990's as well as looking towards the frontier of today and the expected applications it will create for tomorrow.

Three historical eras have been identified with distinct paradigms; the Voice era, the Entertain me era and the Connect me era. A fourth one, the Anywhere era, is being established right now where services will be available anywhere and where everything and anything will be connected.

The paper outlines the technical and economical trends in the Anywhere era that influence the wireless applications

over the next coming years and its implications on the industry.

Dr. Martin Zander is Director and Head of Portfolio Management at ST-Ericsson. He has been working in the Telecom Industry since 1999 in strategic product management as well as sales & marketing with mobile phones, mobile platforms, and multimedia service layer products. Between 2003 and 2006, he was responsible for setting up and managing Ericsson Mobile Platforms product marketing activities in Japan. After returning to Europe, Mr. Zander joined Ericsson Multimedia division where he managed their service layer and multimedia portfolio and thereafter he joined ST-Ericsson in 2009.

FDSOI: From Materials to Devices and Circuit Applications

Dr. Carlos Mazuré, SOITEC

Carlos Mazuré, SOITEC France
Richard Ferrant, SOITEC France
Bich-Yen Nguyen, SOITEC France
Walter Schwarzenbach, SOITEC France
Cécile Moulin, SOITEC France

Abstract
Nanotechnology starts at the substrate level. The SOI substrates enable performance improvement, area saving and power reduction for ICs through a convolution of substrate design and device architecture to maximize the benefits at the IC level. SOI substrates have made possible an efficient PDSOI MOSFET optimization increasing current drive while minimizing leakage and reducing parasitic elements. Further development of the SOI substrate technology has made possible to position ultra thin silicon SOI (UTSOI) as an industrial option for the manufacturing of FDSOI device architectures where the SOI film thickness uniformities is controlled below ±5A across the wafer and wafer to wafer. FDSOI enables the design for low power and high performance IC products. FDSOI circuit design does not have to take into consideration the history effect of PDSOI nor the high threshold voltage variation due to random dopant fluctuation given that the transistor channels are undoped. This makes the porting of designs from bulk to FDSOI much simpler. An overview of the advances in Smart Cut UTSOI and FDSOI devices and circuit applications will be given.

Dr. Carlos Mazuré, Chief Technology Officer, Executive Vice President of Soitec Group is involved in defining Soitec's technology strategy and leads advanced technology alliances with customers and academia. He focuses on assessing the device-substrate system, in the understanding of the advantages that SOI and engineered substrates bring to the device architecture, and in the development of innovative SOI based circuit solutions. He works closely with R&D, Business Units, Business Development, Sales and customers to help support existing technology programs and open new applications. He joined Soitec in 2001 to create the R&D organization, which he directed until 2009.

Prior to joining Soitec, Dr. Mazure worked for Infineon Technologies in Munich, Germany, where he headed the ferroelectric FeRAM development program. Later, as Director of Business Development at Infineon he initiated the Infineon-Toshiba FeRAM Development Alliance. Before moving to Germany, he worked for the IBM/Infineon DRAM Development Alliance in East Fishkill, New York. His experience also includes work on SOI, BiCMOS high performance SRAM and technology development at APRDL, Motorola Semiconductor in Austin, Texas.

Mazure holds two doctorates in physics, one from the Grenoble University, France, and the other from the Technical University of Munich, Germany. He has authored or co-authored more than 150 technical papers and holds more than 90 patents worldwide. He is a member of the Semiconductor Advisory Board of Virginia Tech, member of several international technology and advisory committees, IEEE senior member and a regular invited speaker at international conferences and workshops.

TERAHERTZ IMAGING WITH CMOS/BICMOS PROCESS TECHNOLOGIES

Dr. Ullrich Pfeiffer, Univ. of Wuppertal, Germany

Ullrich Pfeiffer, Univ. of Wuppertal, Germany
Erik Öjefors, Univ. of Wuppertal, Germany

Abstract

Contrary to the common belief, silicon devices may very well operate beyond their cut-off frequency. The push towards terahertz frequencies, though, presents both challenges and opportunities for emerging applications. This paper summarizes recent attempts to use foundry-level silicon process technologies for the realization of terahertz electronic systems.

Dr. Ullrich R. Pfeiffer received the diploma degree in physics and the Ph.D. in physics from the University of Heidelberg, Germany, in 1996 and 1999, respectively. In 1997 he worked as a research fellow at the Rutherford Appleton Laboratory, Oxfordshire England. In 2000 his research was on real-time electronics for a LHC-Experiment at the European Organization for Nuclear Research (CERN), Switzerland. From 2001 to 2006 he was with the IBM T.J. Watson Research Center where his research involved RF circuit design, power amplifier design at 60GHz and 77GHz, high-frequency modeling and packaging for mmWave communication systems. In 2007 he received an European Young Investigator Award and lead the THz electronics group at the Institute of High-Frequency and Quantum Electronics at the University of Siegen, Germany. Since 2008 he holds the High-frequency and Communication Technology chair at the University of Wuppertal, Germany. Dr. Pfeiffer was the co-recipient of the 2004 and 2006 Lewis Winner Award for Outstanding Paper at the IEEE International Solid-State Circuit Conference, the co-recipient of the 2006 IBM Pat Goldberg Memorial Best Paper Award, the 2008 EuMIC Best Paper Award, and the 2009 Best RFIC Oral Paper Award.

ANALOG MIXED-SIGNAL CIRCUITS IN ADVANCED NANO-SCALE CMOS TECHNOLOGY FOR MICRO-PROCESSORS AND SOCS

Dr. Ian A. Young, INTEL Corp.

Abstract

Scaling of CMOS technology has made major innovations in the last decade with the introduction of strained silicon and high-k metal gate, however at the same time an increasing amount of complex analog mixed-signal circuit functionality has been integrated on microprocessors and SOCs.

Examples of the key analog mixed-signal circuit functional blocks implemented in advanced 45nm and 32nm logic CMOS on microprocessors and SOCs are described. Techniques that overcome the challenges of the low supply voltage and dimensional scaling in 45 nm and 32nm CMOS include the use of the digital transistor for analog circuits, the use of “digital assist” logic for calibration and differential pair offset cancellation. The co-optimization of design techniques and process enhancements for high performance RF wireless circuits integrated on SOCs was employed to manage complexity and cost.

Dr. Ian A. Young received the BSEE and the M. Eng. Science from the University of Melbourne, Australia. He received the Ph.D in Electrical Engineering from the University of California, Berkeley. He joined Intel Corporation in 1983 where he is a Senior Fellow in the Technology and Manufacturing Group. He is a Fellow of the IEEE.

His technical contributions at Intel have been in the design of DRAMs, SRAMs, microprocessor circuit design, Phase Locked Loops for microprocessor clocking, mixed-signal circuits for microprocessor high speed I/O links, and RF CMOS circuits for wireless. He has also contributed to the definition and development of Intel's process technologies. Until recently he was directing the research and development of analog mixed signal and RF circuits in 32nm and 22nm logic processes. He now leads a research group exploring the future directions for the integrated circuit in the post CMOS era.

He was a member of the Symposium on VLSI Circuits Technical Program Committee from 1991 to 98 serving as the Symposium Chairman in 1998. He was a member of the ISSCC Technical Program Committee from 1992 to 2005 and Chair of the Technical Program Committee in 2005. He currently serves on the Solid-State Circuits Society Adcom.

ULTRA LOW POWER AND MINIATURIZED MEMS-BASED RADIO FOR BAN AND WSN APPLICATIONS

Dr. David Ruffieux, Swiss Center for Electronics and Microtechnology (CSEM)

David Ruffieux, Swiss Center for Electronics and Microtechnology (CSEM), Switzerland
Matteo Contaldo, Swiss Center for Electronics and Microtechnology (CSEM), Switzerland
Jérémie Chabloz, Swiss Center for Electronics and Microtechnology (CSEM), Switzerland
Christian Enz, Swiss Center for Electronics and Microtechnology (CSEM), Switzerland

Abstract

This paper explores where MEMS devices such as BAW and low frequency silicon resonators can be used to reach further miniaturization and to lower the power dissipation of 2.4GHz transceivers targeting BAN and WSN applications. The system requirements for improving such networks are derived after analyzing appropriate low power communication protocols. A super-heterodyne transceiver architecture taking advantages of the high-Q of BAW resonators to reach lower phase noise and implement highly selective RF filters to reject interferers or unwanted IF harmonics is then presented. The design of related MEMS-based specific circuits is also discussed in details. Experimental results validate the functioning of the complete transceiver in both RX and TX modes. The measurements also demonstrate phase locking of the synthesizer to an electronically temperature-compensated low frequency silicon resonator, which is used to implement a unique ultra-low power oscillator for both RTC and reference frequency functions. Key measured features are a phase noise of -140dBc/Hz at 1MHz offset and the demonstration of 1Mbps GFSK modulation in TX. The receiver sensitivity reaches only -66dBm at 200kbps requiring further investigations to understand the reasons of the current limitation.

Dr. David Ruffieux received the MS and PhD degrees in micro-engineering from the Swiss Federal Institute of Technology (EPFL) and University of Neuchâtel, Switzerland in 1995 and 2000 respectively. In 1995, he was hired by the Swiss Center for Electronics and Microtechnology (CSEM), where he worked in the fields of MEMS and IC design. In

2000, he joined the RF and Analog IC design group of CSEM where he is involved in analog and RF low power, low voltage circuit design. He is now leading research activities in the fields of MEMS-based wireless transceivers and low power RTC based on silicon MEMS resonators. Dr. Ruffieux has authored or co-authored over 15 technical publications and holds 8 patents in his diverse fields of expertise. He was the recipient of the ESSCIRC 1999 best paper award.

MONDAY SEPTEMBER 13TH, 2010

TUTORIAL 1: FILTER DESIGN

Organiser: Andreia Cathelin, STMicroelectronics

Co-organiser: Bram Nauta, University of Twente

Full-Day Tutorial **(9:30 - 16:45)**

Room C

Agenda

9:30-10:30
General introduction on filter design + active RC
Bill Redman-White (NXP and Southampton University)

10:30-11:00 Coffee Break

11:00-12:00

Gm-C filters + noise & power trade-offs in analog filters
Bram Nauta (University of Twente)

12:00-13:00

Tuning and reconfiguration for analog filters
Andreia Cathelin (STMicroelectronics)

13:00-14:30 Lunch

14:30-15:30
Digital filter design
Markus Helfenstein (ST-Ericsson)

15:30-15:45 Coffee Break

15:45-16:45
Switched-cap filters design
Diego Vázquez García de la Vega (University of Seville)

TUTORIAL 2: DESIGN TECHNIQUES FOR HIGH PERFORMANCE CONTINUOUS-TIME DELTA-SIGMA CONVERSION

Shanti Pavan, Indian Institute of Technology, Madras

Half-Day Tutorial **(9:30 - 13:00)**

Room F

Keywords
Oversampling, analogtodigital converters, ADC, mixedsignal design, Continuoustime sigmadelta, multi bit converters, dynamic element matching, noise shaping.

Detailed Tutorial Program

Topics to be covered:

(i) Quick review of the basics of Continuoustime Delta Sigma Modulation

(ii) Problems with continuoustime modulators:

(a) Excess Loop Delay – recent advancements and techniques for compensation.

(b) Clock Jitter – recent developments and techniques to minimize effect of jitter.

(c) Systematic Design Centering – Determining coefficients in a robust and reliable way when practical opamps/ transconductors are considered.

(d) Loop filter Nonlinearity: Understanding loop filter nonlinearities and their effects on CTDSM performance. Techniques to rapidly simulate nonlinearity.

(e) Mitigation of Nonlinearity: Circuit techniques to enhance the linearity of CTDSMs with reduced power dissipation – opamp design considerations, and the "assisted" opamp technique.

(iii) Case Studies:

(a) Low Power, High Resolution Single Bit and Multibit Modulators for Audio.

(b) High speed, 15 MHz bandwidth CTDSM with medium resolution in 0.18um CMOS.

Dr. Shanthi Pavan

Shanthi Pavan obtained the B.Tech degree in Electronics and Communication Eng from the Indian Institute of Technology, Madras in 1995 and the M.S and Sc.D degrees from Columbia University, New York in 1997 and 1999 respectively. From 1997 to 2000, he was with Texas Instruments in Warren, New Jersey, where he worked on high speed analog filters and data converters. From 2000 to June 2002, he worked on microwave ICs for data communication at Bigbear Networks in Sunnyvale, California. Since July 2002, he has been with the Indian Institute of TechnologyMadras, where he is now a Professor of Electrical Engineering. His research interests are in the areas of high speed analog circuit design and signal processing.

Dr. Pavan is the recipient of the IEEE Circuits and Systems Society Darlington Best Paper Award (2009), the Swarnajayanthi Fellowship (from the Government of India), the Young Faculty Recognition Award from IIT Madras (for excellence in teaching), the Technomentor Award from the India Semiconductor Association and the Young Engineer Award from the Indian National Academy of Engineering (2006). Dr.Pavan is

an Associate Editor of the IEEE Transactions on Circuits and Systems: Part I Regular Papers, and earlier served on the editorial board of the IEEE Transactions on Circuits and Systems Part II Express Briefs from 2006-2007.

He is the coauthor (along with Yannis Tsividis) of the book High Frequency Continuous Time Filters in Digital CMOS Processes. (Kluwer, 2001)

Tutorial 3: RF System Design for Advanced Wireless Transceivers

Dr. Lydi Smaïni, RF System Design Manager, Marvell Semiconductor

Half-Day Tutorial **(14:30 - 17:45)**

Room F

Abstract

With growing complexity of wireless communication systems and increasing levels of integration in modern CMOS processes, the differentiation of competing wireless transceiver designs has moved from the transistor-level design to the architectural level. Designing such integrated transceivers requires a thorough understanding of the whole transceiver chain, from the antenna to the DSP. While transistor-level design is taught in most graduate classes, RF system-level design expertise is dominantly acquired through hands-on design work, with sometimes missing theoretical background. This tutorial provides the attendance with practical RF system-design knowledge directly applicable to their ongoing transceiver design.

Dr. Lydi Smaïni

Dr. Smaïni received his M.S. and Ph.D. degrees in Electronics from the University of South Toulon-Var, France, in 1998 and 2001, respectively, specializing in Radio Propagation, Telecommunications and Remote Sensing. His thesis work focused on pulse compression techniques and signal processing for atmospheric radars. After graduation he worked for one year as an R&D consulting engineer for ALTEN, Marseille, France, where he developed a frequency agile radar beacon for navigation aid, which is now in service on the French littoral. From 2002 to 2006 he was with STMicroelectronics in the RF System and Architecture Group for wireless communications, Geneva, Switzerland, where he worked on Ultra Wide-Band impulse radio, 3G cellular

phones, and advanced radio architectures for OFDMA technology. He joined Marvell Switzerland in July 2006, Etoy, Switzerland, where he is currently leading the RF System and DSP Team working on deep sub-micron CMOS transceivers.

For further information about these tutorials, please visit the webpage of the conference at http://www.esscirc2010.org/esscircTut.html

Analog Voltage References
(Lecture)

Session Code: A3L-F

Location: Room A

Date & Time: Tuesday September 14, 2010
(11:20 - 13:00)

Chair(s): Doug Smith,
SMSC, UK
Andrei Vladimirescu,
University of California Berkeley, USA

11:20 **A 65-nm CMOS Temperature-Compensated Mobility-Based Frequency Reference for Wireless Sensor Networks**
Fabio Sebastiano, Lucien Breems, *NXP Semiconductors.* Kofi Makinwa, TU *Delft.* Salvatore Drago, Domine Leenaerts, *NXP Semiconductors.* Bram Nauta, *University of Twente.*

11:40 **A Temperature Compensation Word-Line Voltage Generator for Multi-Level Cell NAND Flash Memories**
Toru Tanzawa, Tomoharu Tanaka, Satoru Tamada, Jiro Kishimoto, Shigekazu Yamada, Koichi Kawai, Takaaki Ichikawa, *Micron Japan Ltd.* Pin-Chou Chiang, Frankie Roohparvar, *Micron Technology Inc.*

12:00 **Variability Analysis of a Digitally Trimmable Ultra-Low Power Voltage Reference**
Mingoo Seok, Gyouho Kim, David Blaauw, Dennis Sylvester, *University of Michigan.*

12:20 **A Nano-Ampere Current Reference Circuit and its Temperature Dependence Control by using Temperature Characteristics of Carrier Mobilities**
Tetsuya Hirose, Yuji Osaki, Nobutaka Kuroki, Masahiro Numa, *Kobe University.*

12:40 **A High PSRR Class-D Audio Amplifier IC Based on a Self-Adjusting Voltage Reference**
Alexandre Huffenus, Gaël Pillonnet, Nacer Abouchi, *University of Lyon.* Frédéric Goutti, Vincent Rabary, Robert Cittadini, *ST Microelectronics.*

TUESDAY SEPTEMBER 14

Imagers
(Lecture)

Session Code:	A3L-G
Location:	Room C
Date & Time:	Tuesday September 14, 2010 (11:20 - 13:00)
Chair(s):	Werner Brockherde, *Fraunhofer IMS, Germany* Robert Henderson, *University of Edinburgh, UK*

11:20 **A 160x120-Pixel Uncooled IR-FPA Readout Integrated Circuit with on-Chip Non-Uniformity Compensation**
Matteo Perenzoni, Daniel Mosconi, David Stoppa, FBK Fondaziones *Bruno Kessler.*

11:40 **An Ultra-Low Power Current-Mode CMOS Image Sensor with Energy Harvesting Capability**
Fang Tang, Yuan Cao, Amine Bermak, *The Hong Kong University of Science and Technology.*

12:00 **Large Full-Well Capacity Stitched CMOS Image Sensor for High Temperature Applications**
Daniel Durini, Frank Matheis, Christian Nitta, Werner Brockherde, Bedrich Hosticka, *Fraunhofer IMS.*

12:20 **A 100dB Dynamic Range Event-Driven Spatial Contrast Sensor with 100us Response Time and Time-to-First-Spike Mode**
Juan Antonio Leñero-Bardallo, Teresa Serrano-Gotarredona, Bernabe Linares-*Barranco, IMSE-CNM-CSIC.*

12:40 **A 30µW 100dB Contrast Vision Sensor with Sync-Async Readout and Data Compression**
Nicola Massari, Marco De Nicola, Massimo Gottardi, *FBK Fondaziones Bruno Kessler.*

TUESDAY SEPTEMBER 14

RF Frequency Synthesis
(Lecture)

Session Code: A3L-H

Location: Room F

Date & Time: Tuesday September 14, 2010 (11:20 - 13:00)

Chair(s): Roc Berenguer, *CEIT, Spain*
Antonio Liscidini, *University of Pavia, Italy*

11:20 **A 1.7-mW Dual-Band CMOS Frequency Synthesizer for Low Data-Rate Sub-GHz Applications**
Calogero Marco Ippolito, Alessandro Italia, Giuseppe Palmisano, *Universita di Catania.*

11:40 **A Transmitter CMOS VCO for WCDMA/EDGE**
Pietro Andreani, *Lund University/ST-Ericsson.* Kirill Kozmin, Per Sandrup, Thomas Mattsson, *ST-Ericsson.*

12:00 **A 4.1 to 5.1GHz 430µA Injection-Locked Frequency Divider by 7 in 65nm CMOS**
Andrea Bevilacqua, *University of Padova.* Leonardo Lorenzon, *University of Padova, Infineon Technology.* Nicola Da Dalt, *Infineon Technology.* Andrea Gerosa, Andrea Neviani, *University of Padova.*

12:20 **An Automatic Frequency Calibration Technique for Fractional-N Frequency Synthesizers**
Shih-Hao Tarng, Jia-Hung Peng, Tzu-Chan Chueh, Ming-Ching Kuo, *Industrial Technology Research Institute, Taiwan.*

12:40 **A 0.9mW PLL Integrated in an Ultra-Low-Power SoC for WPAN and WBAN Applications**
Gabriele Devita, Alan Chi Wai Wong, Nikolao Kasparidis, Phil Corbishley, Alison Burdett, Paul Paddan, *Toumaz Technology LTD.*

TUESDAY SEPTEMBER 14

Amplifiers I
(Lecture)

Session Code:	A5L-F
Location:	Room A
Date & Time:	Tuesday September 14, 2010 (15:50 - 16:50)
Chair(s):	Markus Helfenstein, *ST Ericsson, Switzerland* Peter Mole, *Intersil, UK*

15:50 **Low Distortion Active Filters Using the Gm-Assisted OTA-RC Technique**
Siva Thyagarajan, *University of California, Berkeley.* Shanthi Pavan, Prabu Sankar, *Indian Institute of Technology, Madras.*

16:10 **A High-Linearity Low-Noise Reconfiguration-Based Programmable Gain Amplifier**
Huy-Hieu Nguyen, Hoai-Nam Nguyen, Jeong-Seon Lee, Sang-Gug Lee, *KAIST.*

16:30 **A 1.8µW 1uV-Offset Capacitively-Coupled Chopper Instrumentation Amplifier in 65nm CMOS**
Qinwen Fan, *TU Delft.* Fabio Sebastiano, *NXP.* Kofi Makinwa, Han Huijsing, *TU Delft.*

Micropower AD Interfaces
(Lecture)

Session Code: A5L-G

Location: Room C

Date & Time: Tuesday September 14, 2010
(15:50 - 16:50)

Chair(s): Kofi Makinwa,
TU Delft, Netherlands
Willy Sansen,
KU Leuven, Belgium

15:50 **Subthreshold Current-Mode Oscillator-Based Quantizer with 3-Decade Scalable Sampling Rate and Pico-Ampere Range Resolution**
Armin Tajalli, Yusuf Leblebici, EPFL *Ecole Polytechnique Federale de Lausanne.*

16:10 **An All-Digital A/D Converter TAD with 4-Shift-Clock Construction for Sensor Interface in 0.65-µm CMOS**
Takamoto Watanabe, Tomohito Terasawa, *DENSO Corporation.*

16:30 **All-Digital on-Chip Monitor for PMOS and NMOS Process Variability Measurement Utilizing Buffer Ring with Pulse Counter**
Tetsuya Iizuka, Jaehyun Jeong, Toru Nakura, Makoto Ikeda, Kunihiro Asada, *University of Tokyo.*

TUESDAY SEPTEMBER 14

mm-Wave Transceivers
(Lecture)

Session Code: A5L-H

Location: Room F

Date & Time: Tuesday September 14, 2010 (15:50 - 16:50)

Chair(s): Didier Belot, *ST Microelectronics, France*
Piet Wambacq, *IMEC, Belgium*

15:50 **Low-Power Fully-Integrated K-Band Transceiver Using Transformer Direct-Stacking/Connecting and Balun Signal-Combining Techniques**
Nobuhiro Shiramizu, Akihiro Nakamura, Takahiro Nakamura, Toru Masuda, Katsuyoshi Washio, *Hitachi Ltd.*

16:10 **A 45-67GHz UWB Transmitter with >8dBm Output Power for Indoor Radar Applications**
Hugo Veenstra, Marc Notten, *Philips Research.* Dixian Zhao, John Long, TU *Delft.*

16:30 **A 17-Tap 3.5 Gbps Finite Impulse Response Pulse Shaping Filter for 60 GHz Transmitter with QPSK Modulation**
Jinshu Zhao, Marcus Hellfeld, Thomas Wolf, *Dresden University of Technology.* Le Ye, *Pekin University.* Frank Ellinger, *Dresden University of Technology.*

Cryptographic Processors
(Lecture)

Session Code: A6L-E

Location: Room D

Date & Time: Tuesday September 14, 2010
(17:20 - 18:40)

Chair(s): Doris Schmitt-Landsiedel,
TU München, Germany
Hannu Tenhunen,
Royal Institute of Technology KTH, Sweden

17:20 **3GHz, 74mW 2-Level Karatsuba 64b Galois Field Multiplier for Public-Key Encryption Acceleration in 45nm CMOS**
Sanu Mathew, Mike Kounavis, Farhana Sheikh, Steven Hsu, Amit Agarwal, Himanshu Kaul, Mark Anders, Frank Berry, Ram Krishnamurthy, *Intel Corp.*

17:40 **FPGA Parallel Pipelined AES-GCM Core for 100G Ethernet Applications**
Luca Henzen, Wolfgang Fichtner, IIS, *ETH Zurich.*

18:00 **A 521-Bit Dual Field Elliptic Curve Cryptograhic Processor with Power Analysis Resistance**
Jen-Wei Lee, Yao-Lin Chen, Chih-Yeh Tseng, Hsie-Chia Chang, Chen-Yi Lee, *National Chiao Tung University.*

18:20 **18Gbps, 50mW Reconfigurable Multi-Mode SHA Hashing Accelerator in 45nm CMOS**
Rajaraman Ramanarayanan, Sanu Mathew, Farhana Sheikh, Suresh Srinivasan, Amit Agarwal, Steven Hsu, Himanshu Kaul, Mark Anders, Vasantha Erraguntla, Ram Krishnamurthy, *Intel Corp.*

TUESDAY SEPTEMBER 14

SAR ADCs and DACs
(Lecture)

Session Code: A6L-F

Location: Room A

Date & Time: Tuesday September 14, 2010 (17:20 - 18:40)

Chair(s): Klaas Bult, *Broadcom, Netherlands*
Piero Malcovati, *University of Pavia, Italy*

17:20 **A 12fJ/Conversion-Step 8bit 10MS/s Asynchronous SAR ADC for Low Energy Radios**
Pieter Harpe, Cui Zhou, Xiaoyan Wang, Guido Dolmans, Harmke de Groot, *Holst Centre - IMEC Netherlands.*

17:40 **An 11b 60MS/s 2.1mW Two-Step Time-Interleaved SAR-ADC with Reused S&H**
Sai-Weng Sin, Li Ding, Yan Zhu, He-Gong Wei, Chi-Hang Chan, U-Fat CHIO, Sen-Pang U, Rui Paulo Martins, *University of Macau.* Franco Maloberti, *University of Pavia.*

18:00 **A 1.8-V 12-Bit 250-MS/s 25-mW Self-Calibrated DAC**
Jen-Hung Chi, Shih-Hsuan Chu, Tsung-Heng Tsai, *National Chung Cheng University.*

18:20 **A 94dB-SNR -76dB-THD High-Efficiency Hybrid Audio Power-DAC for Loudspeaker (4Ohm/8Ohm) and Earphone (16Ohm/32Ohm)**
Andrea Baschirotto, *University of Milano-Bicocca.* Giacomino Bollati, Vittorio Colonna, Gabriele Gandolfi, *Marvell.*

Power Management
(Lecture)

Session Code: A6L-G

Location: Room C

Date & Time: Tuesday September 14, 2010
(17:20 - 18:40)

Chair(s): Ralf Brederlow,
Texas Instruments, Germany
Frank Op 't Eynde,
Audax-Technologies Ltd, Belgium

17:20 **A Photovoltaic System with an Analog Maximum Power Point Tracking Technique for 97.3% High Effectiveness**
Chun-Yu Hsieh, Chih-Yu Yang, Fu-Kuei Feng, Ke-Horng Chen, *NCTU National Chiao Tung University.*

17:40 **An Electro-Magnetic Energy Harvester with 190nW Idle Mode Power Consumption for Wireless Sensor Nodes**
Hannes Reinisch, *Graz University of Technology.* Stefan Gruber, Martin Wiessflecker, *Infineon Technologies Austria AG.* Hartwig Unterassinger, *Graz University of Technology.* Günter Hofer, *Infineon Technologies Austria AG.* Wolfgang Pribyl, *Graz Univ. of Technology.* Gerald Holweg, *Infineon Technologies Austria AG.*

18:00 **An Integrated 120 Volt AC Mains Voltage Interface in Standard 130 nm CMOS**
Andres Tamez, Jeffrey Fredenburg, Michael P. Flynn, *University of Michigan.*

18:20 **A 9 pW/Hz Adjustable Clock Generator with 3-Decade Tuning Range for Dynamic Power Management in Subthreshold SCL Systems**
Armin Tajalli, Yusuf Leblebici, *EPFL Ecole Polytechnique Federale de Lausanne*.

TUESDAY SEPTEMBER 14

mm-Wave Frequency Generation
(Lecture)

Session Code: A6L-H

Location: Room F

Date & Time: Tuesday September 14, 2010 (17:20 - 18:40)

Chair(s): Jan Craninckx, *IMEC, Belgium*
Marc Tiebout, *Infineon, Austria*

17:20 **A 60GHz 15.7mW Static Frequency Divider in 90nm CMOS**
Lianming Li, Patrick Reynaert, Michiel Steyaert, *KU Leuven, ESAT-MICAS.*

17:40 **A Comparison Between Grounded and Floating Shield Inductors for mmW VCOs**
Jose Luis González Jimenez, Xavier Aragones, Marc Molina*, UPC Universitat Politecnica de Catalunya.* Baudouin Martineau, Didier Belot, *STMicroelectronics.*

18:00 **A 40 nm LP CMOS PLL for High-Speed mm-Wave Communication**
Bertrand Parvais, Karen Scheir, Vojkan Vidojkovic, Roeland Vandebriel, *IMEC.* Gerd Vandersteen, *VUB Vrije Universiteit Brussel.* Charlotte Soens*, IMEC.* Piet Wambacq, *IMEC/VUB.*

18:20 **A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c TRX**
David Murphy, Qun Jane Gu, Yi-Cheng Wu, Heng-Yu Jian, Zhiwei Xu, Adrian Tang, Frank Wang, *UCLA.* Yu-Ling Lin, Ho-Hsiang Chen, Chewnpu Jou, *TSMC.* Mau-Chung Frank Chang, *UCLA.*

TDCs and Timing Circuits
(Lecture)

Session Code: B3L-F

Location: Room A

Date & Time: Wednesday September 15, 2010 (11:20 - 13:00)

Chair(s): Rui Martins, *University of Macau, Macau*
Paul Muller, *Mediatek, UK*

11:20 **Time-to-Digital Converter with 3-ps Resolution and Digital Linearization Algorithm**
Marco Zanuso, Salvatore Levantino, Alberto Puggelli, Carlo Samori, Andrea Lacaita, *Politecnico de Milano.*

11:40 **Time-to-Digital Converter Based on Time Difference Amplifier with Non-Linearity Calibration**
Shingo Mandai, Tetsuya Iizuka, Toru Nakura, Makoto Ikeda, Kunihiro Asada, *The University of Tokyo.*

12:00 **All Digital Modulation Bandwidth Extension Technique for Narrow Bandwidth Analog Fractional-N PLL**
Ping-Ying Wang, Chia-Huang Fu, *Mediatec.*

12:20 **Ultra Low Power RC Oscillator for System Wake-Up Using Highly Precise Auto-Calibration Technique**
Joonhyung Lim, Kwangmook Lee, Koonshik Cho, *Samsung Electro-Mechanics.*

12:40 **A 500mV 650pW Random Number Generator in 130nm CMOS for a UWB Localization System**
Christophe De Roover, Michiel Steyaert, *KU Leuven.*

ESSCIRC PROGRAMME

WEDNESDAY SEPTEMBER 15

Sensors
(Lecture)

Session Code: B3L-G

Location: Room C

Date & Time: Wednesday September 15, 2010
(11:20 - 13:00)

Chair: Christoph Hagleitner,
IBM Zurich, Switzerland
Michiel Pertijs,
TU *Delft, Netherlands*

11:20 **A 0.12mm^2 7.4µW Micropower Temperature Sensor with an Inaccuracy of ±0.2°C (3-Sigma) from -30°C to 125°C**
Kamran Souri, Kofi Makinwa, *TU Delft.*

11:40 **A 4.3 mm^2 ASIC for a 300 °/s 2-Axis Capacitive Micro-Gyroscope**
Lasse Aaltonen, Antti Kalanti, Mika Pulkkinen, Matti Paavola, Mika Kämäräinen, Kari Halonen, *Aalto University.*

12:00 **An Interface for Eddy Current Displacement Sensors with 15-Bit Resolution and 20 MHz Excitation**
Mohammad Reza Nabavi, Michiel Pertijs, Stoyan Nihtianov, TU *Delft.*

12:20 **A 160x120-Pixels Range Camera with on-Pixel Correlated Double Sampling and Nonuniformity Correction in 29.1µm Pitch**
Matteo Perenzoni, Nicola Massari, David Stoppa, Lucio Pancheri, Mattia Malfatti, Lorenzo Gonzo, *FBK Fondazione Bruno Kessler.*

12:40 **Range Finding Sensor in 90nm CMOS with Bridge Correlator Based Background Light Suppression**
Milos Davidovic, *Vienna University of Technology.* Gerald Zach, *RIEGL Laser Measurement Systems GmbH*. Kerstin Schneider-Hornstein, Horst Zimmermann, *Vienna University of Technology.*

Power amplifiers
(Lecture)

Session Code: B3L-H

Location: Room F

Date & Time: Wednesday September 15, 2010 (11:20 - 12:40)

Chair(s): Yorgos Palaskas, *Intel, USA*
Ullrich Pfeiffer, *University of Wuppertal, Germany*

11:20 **A 2.4 GHz Fully Integrated Doherty Power Amplifier Using Series Combining Transformer**
Ercan Kaymaksüt, Patrick Reynaert, *KU Leuven.*

11:40 **A Higly Linear 25dBm Outphasing Power Amplifier in 32nm CMOS for WLAN Application**
Hongtao Xu, Yorgos Palaskas, Ashoke Ravi, Krishnamurthy Soumyanath, *Intel Corporation.*

12:00 **A Class-D Outphasing RF Amplifier with Harmonic Suppression in 90nm CMOS**
Jonas Fritzin, Christer Svensson, Atila Alvandpour, *Linköping University.*

12:20 **60GHz Power Amplifier with Distributed Active Transformer and Local Feedback**
Ying He, Lianming Li, Patrick Reynaert, *ESAT-MICAS, KU Leuven.*

WEDNESDAY SEPTEMBER 15

Amplifiers II
(Lecture)

Session Code: B5L-F

Location: Room A

Date & Time: Wednesday September 15, 2010
(15:50 - 16:50)

Chair(s): Marco Berkhout,
NXP, Netherlands
Franz Dielacher,
Infineon, Austria

15:50 **A Low-Power Orthogonal Current-Reuse Amplifier for Parallel Sensing Applications**
Ben Johnson, David DeTomaso, Alyosha Molnar, *Cornell University.*

16:10 **200 µW CMOS Class AB Unity-Gain Buffers with Accurate Quiescent Current Control**
Antonio J. Lopez-Martin, Jose M. Algueta, *Public University of Navarra.* Lucia Acosta, *University of Sevilla.* Jaime Ramirez-Angulo, *New Mexico State University.* Ramon G. Carvajal, *University of Sevilla.*

16:30 **A 470 µW Clock-Free Current-Controlled Class D Amplifier with 0.02% THD+N and 82dB PSRR**
Joselyn Torres, Adrian Colli-Menchi, Miguel Angel Rojas-González, Edgar Sánchez-Sinencio, *Texas A&M University.*

Circuits for Implantable Devices
(Lecture)

Session Code: B5L-G

Location: Room C

Date & Time: Wednesday September 15, 2010
(15:50 - 16:50)

Chair(s): Andreas Demosthenous,
UCL University College London, UK
Manuel Delgado-Restituto,
IMSE-CNM-CSIC, Spain

15:50 **A Multi-Channel Low-Power IC for Neural Spike Recording with Data Compression and Narrow-band 400-MHz MC-FSK Wireless Transmission**
Andrea Bonfanti, Maria Ceravolo, Guido Zambra, Riccardo Gusmeroli, Tommaso Borghi, Alessandro Sottocornola Spinelli, Andrea Leonardo Lacaita, *Politecnico di Milano.*

16:10 **Micropower Integrated Bioamplifier and Auto-Ranging ADC for Wireless and Implantable Medical Instrumentation**
Yu Chi, Gert Cauwenberghs, *UCSD.*

16:30 **A DC-Isolated Fine-Controlled Neural Stimulator**
Xiao Liu, Andreas Demosthenous, Nick Donaldson, *University College London.*

WEDNESDAY SEPTEMBER 15

mm-Wave Receivers
(Lecture)

Session Code: B5L-H

Location: Room F

Date & Time: Wednesday September 15, 2010 (15:50 - 16:50)

Chair(s): Andreas Kaiser, *IEMN, France*
Bram Nauta, *University of Twente, Netherlands*

15:50 **A 24 dB Gain 51-68 GHz CMOS Low Noise Amplifier Using Asymmetric-Layout Transistors**
Ning Li, Keigo Bunsen, Naoki Takayama, Qinghong Bu, *Tokyo Institute of Technology.* Toshihide Suzuki, Masaru Sato, Tatsuya Hirose, *Fujitsu Laboratories Ltd.* Kenichi Okada, Akira Matsuzawa, *Tokyo Institute of Technology.*

16:10 **A 24-GHz 90-nm CMOS Beamforming Receiver Front-End with Analog Baseband Phase Rotation**
Andreas Axholt, Henrik Sjöland, *Lund University.*

16:30 **A Fifth-Order 880MHz/1.76GHz Active Lowpass Filter for 60GHz Communications in 40nm Digital CMOS**
Piet Wambacq, Vito Giannini, Karen Scheir, Wim Van Thillo, *IMEC.* Yves Rolain, *VUB Vrije Universiteit Brussel.*

Memories
(Lecture)

Session Code: B6L-E

Location: Room D

Date & Time: Wednesday September 15, 2010 (17:20 - 18:40)

Chair(s): Jos Huisken,
IMEC-NL/ Holst Centre, Netherlands
Tobias Noll,
RWTH Aachen University, Germany

17:20 **0.5-V, 150-MHz, Bulk-CMOS SRAM with Suspended Bit-Line Read Scheme**
Toshikazu Suzuki, Shinichi Moriwaki, Atsushi Kawasumi, Shinji Miyano, Hirofumi Shinohara, *Semiconductor Technology Academic Research Center*

17:40 **A 4.4pJ/Access 80MHz, 2K Word X 64b Memory with Write Masking Feature and Variability Resilient Multi-Sized Sense Amplifier Redundancy for Wireless Sensor Nodes Applications**
Vibhu Sharma, *KU Leuven & IMEC-NL.* Stefan Cosemans, *KU Leuven & IMEC.* Maryam Ashouei, Jos Huisken, *IMEC-NL.* Francky Catthoor, *IMEC.* Wim Dehaene, *KU Leuven & IMEC.*

18:00 **A 40nm CMOS 260kb SRAM-bitcell on-Chip Failure Monitoring Test Scribe with Integer-to-Current Converter**
Brice Lhomme, Yann Carminati, Bertrand Borot, Olivier Callen, Thierry Burdeau, Sylvain Clerc, *STMicroelectronics.*

18:20 **Crosshairs SRAM - an Adaptive Memory for Mitigating Parametric Failures**
Gregory Chen, Michael Wieckowski, David Blaauw, Dennis Sylvester, *University of Michigan.*

WEDNESDAY SEPTEMBER 15

Pipeline ADCs
(Lecture)

Session Code: B6L-F

Location: Room A

Date & Time: Wednesday September 15, 2010
(17:20 - 18:40)

Chair(s): Patrick Quinn,
Xilinx Dublin, Ireland
Arthur van Roermund,
TU/e Eindhoven, Netherlands

17:20 **A 2.4 GS/s, 4.9 ENOB at Nyquist, Single-Channel Pipeline ADC in 65nm CMOS**
Timmy Sundström, Christer Svensson, Atila Alvandpour, *Linköping University.*

17:40 **A 11.1-Bit ENOB 50-MS/s Pipelined A/D Converter in 130-nm CMOS Without S/H Front End**
Jurg Treichler, Qiuting Huang, *Integrated Systems Laboratory ETH Zurich.*

18:00 **A 12-Bit, 30-MS/s, 2.95-mW Pipelined ADC Using Single-Stage Class-AB Amplifiers and Deterministic Background Calibration**
Justin Kim, Boris Murmann, *Stanford University.*

18:20 **A Reconfigurable 10-12b 0.4-44MS/s Pipelined ADC with 0.35-0.5pJ/Step in 1.2V 90nm Digital CMOS**
Mohammad Taherzadeh-Sani, Anas Hamoui, *McGill University.*

Biomedical applications
(Lecture)

Session Code: B6L-G

Location: Room C

Date & Time: Wednesday September 15, 2010 (17:20 - 18:20)

Chair(s): Kari Halonen, *Aalto University, Finland*
Roland Thewes, *TU Berlin, Germany*

17:20 **Enabling Multiple Robotic Functions in an Endoscopic Capsule for the Entire Gastrointestinal Tract Exploration**
Oscar Alonso, Joan Canals, Lluis Freixas, Josep Samitier, Angel Diéguez, UB *University of Barcelona.* Monica Vatteroni, Ekawahyu Susilo, Carmela Cavallotti, Pietro Valdastri, *Scuola Superiore Sant'Anna.*

17:40 **Digital Potentiostat for Electrochemical Bio Sensor Chips**
Alexander Frey, *Siemens AG.* Philipp Kruppa, TU *München.* Ingo Kuehne, Meinrad Schienle, *Siemens AG.* Norbert Persike, Gerhard Hartwich, *Friz Biochem.* Helmut Seidel, *Saarland University.*

18:00 **A Quadrature Receiver for µNMR Applications in 0.13µm CMOS**
Jens Anders, Paul SanGiorgio, Giovanni Boero, EPFL *Ecole Polytechnique Federale de Lausanne.*

WEDNESDAY SEPTEMBER 15

RF building blocks
(Lecture)

Session Code: B6L-H

Location: Room F

Date & Time: Wednesday September 15, 2010 (17:20 - 18:40)

Chair(s): Pietro Andreani, *University of Lund, Sweden*
Andrea Bevilacqua, *University of Padova, Italy*

17:20 **A 900µW, 3-5GHz Integrated FM-UWB Transmitter in 90nm CMOS**
Nitz Saputra, John R. Long, *TU Delft.* John J. Pekarik, *IBM.*

17:40 **A Sub-3dB NF Voltage-Sampling Front-End with +18dBm IIP3 and +2dBm Blocker Compression Point**
Jonathan Borremans, Gunjan Mandal, Bjorn Debaillie, Vito Giannini, Jan Craninckx, *IMEC.*

18:00 **A 0.1 - 4GHz Resistive Feedback LNA with Feedforward Noise and Distortion Cancelation**
Xiao Wang, Wolfgang Aichholzer, Johannes Sturm, *Carinthia University of Applied Sciences.*

18:20 **Reliability Assessment of Voltage Controlled Oscillators in 32nm High-K Metal Gate Technology**
Florian Raoul Chouard, *TU München.* Michael Fulde, *Infineon Technologies AG Austria.* Doris Schmitt-Landsiedel, *TU Munchen.*

Oversampled ADCs
(Lecture)

Session Code: C3L-F

Location: Room A

Date & Time: Thursday September 16, 2010
(11:20 - 13:00)

Chair(s): Andrea Baschirotto,
University of Lecce, Italy
Luis Hernández,
Carlos III University, Spain

11:20 **A 0.13µm CMOS 0.1-20MHz Bandwidth 86-70dB DR Multi-Mode DT Delta-Sigma ADC for IMT-Advanced**
Thomas Christen, *Advanced Circuit Pursuit (ACP) AG.* Qiuting Huang, *ETH Zurich / Advanced Circuit Pursuit (ACP) AG*

11:40 **A 100kHz-10MHz BW, 78-to-52dB DR, 4.6-to-11mW Flexible SC Sigma-Delta Modulator in 1.2-V 90-nm CMOS**
Alonso Morgado, Rocío del Río, Jose M. de la Rosa, *IMSE-CNM-CSIC/University of Seville.* Lynn Bos, Julien Rickaert, Geert van der Plas, *IMEC.*

12:00 **A Digitally Calibrated 5mW 2MS/s 4th-Order Delta-Sigma ADC in 0.25µm CMOS with 94dB SFDR**
Keith O'Donoghue, *Cypress Semiconductor.* Paul Hurst, Stephen Lewis, *University of California, Davis.*

12:20 **A Configurable Cascaded Continuous-Time Delta-Sigma Modulator with Up to 15MHz Bandwidth**
Jens Sauerbrey, *Infineon Technologies AG.* Matthias Keller, *University of Freiburg.* Jacinto San Pablo Garcia, Georgi Panov, Thomas Piorek, Xianghua Shen, Markus Schimper, *Infineon Technologies AG.* Maurits Ortmanns, *University of Ulm.* Yiannos Manoli, *University of Freiburg.* Rudolf Koch, *Infineon Technologies AG.*

12:40 **A 0.08 mm^2, 7mW Time-Encoding Oversampling Converter with 10 Bits and 20MHz BW in 65nm CMOS**
Enrique Prefasi, Susana Paton, Luis Hernández, *Carlos III University.* Richard Gaggl, *Lantiq.* Andreas Wiesbauer, *Infineon.* Joerg Hauptmann, *Lantiq.*

THURSDAY SEPTEMBER 16

DC/DC Converters
(Lecture)

Session Code:	C3L-G
Location:	Room C
Date & Time:	Thursday September 16, 2010 (11:20 - 13:00)
Chair(s):	Eduard Alarcón, *UPC Universitat Politècnica de Catalunya, Spain* Bernhard Wicht, *Texas Instruments, Germany*

11:20 **A Fully Integrated 74% Efficiency 3.6V to 1.5V 150mW Capacitive Point-of-Load DC/DC-Converter**
Tom Van Breussegem, Michiel Steyaert, *KU Leuven.*

11:40 **An 8W-2Mhz Buck Converter with Adaptive Dead Time Tolerant to Radiation and High Magnetic Field**
Stefano Michelis, *CERN*-EPFL. Bruno Allongue, Georges Blanchot,*CERN.* Simone Buso, *University of Padova.* Federico Faccio,*CERN.* Cristian Fuentes, *CERN-UTFSM Chile.* Alessandro Marchioro, Stefano Orlandi, *CERN.* Stefano Saggini, *Udine University.* Giorgio Spiazzi, *University of Padova.* Maher Kayal, *EPFL.*

12:00 **A Sensor Concept for Minimizing Body Diode Conduction Losses in DC/DC Converters**
Gerhard Maderbacher, *Graz University of Technology.* Christoph Sandner, *Infineon Technologies Austria.* Thomas Jackum, Wolfgang Pribyl, *Graz University of Technology.*

12:20 **A Single-Inductor Multiple Positive and Negative Outputs (SIMPNO) Converter with a Vector Current Control Mode for Electronic Paper Displays (EPDs)**
Yu-Huei Lee, *National Chiao Tung University.* Ming-Hsin Huang, *National Chiao Tung University-*TSMCTaiwan Semiconductor Manufacturing Company. Yu-Nong Tsai, Ming-Yan Fan, Ke-Horng Chen, *National Chiao Tung University.*

12:40 **Efficiency Enhanced Single-Inductor Boost-Inverting Flyback Converter with Dual Hybrid Energy Transfer Media and a Bifurcation Free Comparator**
Se-Won Wang, Young-Jin Woo, Young-Sub Yuk, Gyu-Hyeong Cho, Gyu-Ha Cho, *KAIST.*

THURSDAY SEPTEMBER 16

Wireless Communications
(Lecture)

Session Code:	C3L-H
Location:	Room F
Date & Time:	Thursday September 16, 2010 (11:20 - 13:00)
Chair(s):	Peter Baltus, *TU/e Eindhoven, Netherlands*

11:20 **A 2x2 MIMO Tri-Band Dual-Mode CMOS Transceiver for Worldwide WiMAX/WLAN Applications**
Kyoohyun Lim, Sunki Min, Sanghoon Lee, Jaewoo Park, Kisub Kang, Hwahyeong Shin, Hyunchul Shim, Sechang Oh, Sungho Kim, Jongryul Lee, *FCI Future Communications IC Inc.* Changsik Yoo, *Hanyang University.* Kukjin Chun, *Seoul National University.*

11:40 **A 0.8V 2.4GHz 1Mb/s GFSK RF Transceiver with on-Chip DC-DC Converter in a Standard 0.18µm CMOS Technology**
Paulo Augusto Dal Fabbro, *EPFL-ELab* EPFL. Tindaro Pittorino, Christoph Kuratli, Robert Kvacek, *EM Microelectronic.* Martin Kucera, Frédéric Giroud, *CSEM.* Steve Tanner, Frédéric Chastellain, *EPFL-ESPLAB.* Arnaud Casagrande, *Asulab.* Arthur Descombes, *EM Microelectronic.* Vincent Peiris, *CSEM.* Pierre-André Farine,*EPFL-ESPLAB.* Maher Kayal, *EPFL-ELab.*

12:00 **A 500µW 5Mbps ULP Super-Regenerative RF Front-End**
Maja Vidojkovic, Simonetta Rampu, *IMEC-NL*. Koji Imamura, *Panasonic.* Pieter Harpe, Guido Dolmans, Harmke de Groot, *IMEC-NL*.

12:20 **A 900-MHz Bandwidth Analog Baseband Circuit with 1-dB Step and 30-dB Gain Dynamic Range**
Masahiro Hosoya, Toshiya Mitomo, Osamu Watanabe, *Toshiba Corporation.*

12:40 **A Low-Cost and Low-Power Single-Chip DAB+/Dab/FM Receiver**
J.C Hsu, C.Y Chou, S.W Chang, Albert Tseng, *Keystone Semiconductor Corp.*

THURSDAY SEPTEMBER 16

Emerging Memories
(Lecture)

Session Code:	C5L-E
Location:	Room D
Date & Time:	Thursday September 16, 2010 (15:50 - 16:50)
Chair(s):	Wim Dehaene, *KU Leuven, Belgium* Tobias Noll, *RWTH Aachen University, Germany*

15:50 **0.5V FinFET SRAM with Dynamic Threshold Control of Pass Gates for Salvaging Malfunctioned Bits**
Shin-Ichi O'Uchi, Kazuhiko Endo, Yong-Xun Liu, Tadashi Nakagawa, Takashi Matsukawa, Yuki Ishikawa, Junichi Tsukada, Hiromi Yamauchi, Toshihiro Sekigawa, Hanpei Koike, Kunihiro Sakamato, Meishoku Masahara, *AIST.*

16:10 **A 4 Megabit Carbon Nanotube-based Nonvolatile Memory (NRAM)**
Glen Rosendale, Sohrab Kianian, Monte Manning, Darlene Hamilton, Xue Ming Henry Huang, Karl Robinson, Young Weon Kim, Thomas Rueckes, *Nantero Inc.*

16:30 **A Highly Reliable Multi-cell Antifuse Scheme Using DRAM Cell Capacitors**
Jong-Pil Son, Jin Ho Kim, Woo Song Ahn, Seung Uk Han, Byung-Sick Moon, Churoo Park, Hong-Sun Hwang, Seong-Jin Jang, Joo Sun Choi, Young-Hyun Jun, *SAMSUNG Electronics.* Soo-Won Kim, *Korea University.*

THURSDAY SEPTEMBER 16

mm-wave radar and imaging
(Lecture)

Session Code:	C5L-F
Location:	Room A
Date & Time:	Thursday September 16, 2010 (15:50 - 16:50)
Chair(s):	Jean-Baptiste Begueret, *IMS Laboratory, France* Patrick Reynaert, *KU Leuven, Belgium*

15:50 **Terahertz Imaging Detectors in a 65-nm CMOS SOI Technology**
Erik Öjefors, Neda Baktash, Yan Zhao, Richard Al Hadi, *University of Wuppertal.* Hani Sherry, *STMicroelectronics-University of Wuppertal.* Ullrich R. Pfeiffer, *University of Wuppertal.*

16:10 **Low Power and High Gain Double-Balanced Mixer Dedicated to 77 GHz Automotive Radar Applications**
Andre Mariano, Thierry Taris, Bernardo Leite, Cedric Majek, Yann Deval, Eric Kerhervé, Jean-Baptiste Begueret, *University of Bordeaux.* Didier Belot, *STMicroelectronics.*

16:30 **A 117mW 77GHz Receiver in 65nm CMOS with Ladder Structured Tunable VCO**
Roc Berenguer, *CEIT-Illinois Institute of Technology.* Gui Liu, *Illinois Institute of Technology.* Abe Akhiyat, *Illinois Institute of Technology-Northrop Grumman Corporation.* Keya Kamtikar, Yang Xu, *Illinois Institute of Technology.*

THURSDAY SEPTEMBER 16

UWB Communications
(Lecture)

Session Code:	C5L-H
Location:	Room F
Date & Time:	Thursday September 16, 2010 (15:50 - 16:50)
Chair(s):	Giuseppe Gramegna, *CSR, UK*

15:50 **A 5Mb/S UWB-IR CMOS Transceiver with a 186pJ/b and 150pJ/b TX/RX Energy Request**
Silvia Soldà, Michele Caruso, Andrea Bevilacqua, Andrea Gerosa, Daniele Vogrig, Andrea Neviani, *University of Padova.*

16:10 **A 1 nJ/b 3.2-to-4.7 GHz UWB 50 Mpulses/s Double Quadrature Receiver for Communication and Localization**
Gilles Masson, Dominique Morche, Helene Jacquinot, Pierre Vincent, Francois Dehmas, *CEA-LETI-Minatec.* Stephane Paquelet, Alexis Bisiaux, *Mitsubishi.* Olivier Fourquin, Jean Gaubert, Sylvain Bourdel, *IM2NP.*

16:30 **RF Spectrum Sensing Technique for Cognitive UWB Radio Network**
Muhammad Anis, Maurits Ortmanns, *University of ULM.* Norbert Wehn, *TU Kaiserslautern.*

THURSDAY SEPTEMBER 16

Circuit design in emerging technologies
(Lecture)

Session Code:	C6L-E
Location:	Room D
Date & Time:	Thursday September 16, 2010 (17:20 - 18:40)
Chair(s):	Wim Dehaene, *KU Leuven, Belgium* Ángel Rodríguez-Vázquez, *IMSE-CNM-CSIC, Spain*

17:20 **An organic integrated capacitive DC-DC up-converter**
Hagen Marien, Michiel Steyaert, *KU Leuven*. Soeren Steudel, Peter Vicca, Steve Smout, *IMEC.* Gerwin Gelinck, *HOLST Center/TNO.* Paul Heremans, *IMEC-KU Leuven.*

17:40 **A loading effect insensitive and high precision clock synchronization circuit**
Kai-Wei Hong, Kuo-Hsing Cheng, Chi-Hsiang Chen, Jen-Chieh Liu, Chien-Cheng Chen, *National Central University Taiwan.*

18:00 **Glitch-Induced Within-Die Variations of Dynamic Energy in Voltage-Scaled Nano-CMOS Circuits**
Dina Kamel, Cédric Hocquet, François-Xavier Standaert, Denis Flandre, David Bol, *UCL Catholic University of Louvain.*

18:20 **The detrimental impact of negative celsius temperature on ultra-low-voltage CMOS logic**
David Bol, Cédric Hocquet, Denis Flandre, Jean-Didier Legat, *UCL Université catholique de Louvain.*

THURSDAY SEPTEMBER 16

Signal Processing Platforms
(Lecture)

Session Code:	C6L-F
Location:	Room A
Date & Time:	Thursday September 16, 2010 (17:20 - 18:40)
Chair(s):	José Pineda de Gyvez, *NXP, The Netherlands* Jos Huisken, *IMEC / Holst Centre, Netherlands*

17:20 **An Energy-Efficient Biomedical Signal Processing Platform**
Joyce Kwong, Anantha Chandrakasan, *Massachusetts Institute of Technology*

17:40 **A 757 Mb/s 1.5 mm² 90 nm CMOS Soft-Input Soft-Output MIMO Detector for IEEE 802.11n**
Christoph Studer, Schekeb Fateh, Dominik Seethaler, *ETH Zurich.*

18:00 **A 2.17 mm² 125 mW Reconfigurable SVD Chip for IEEE 802.11n System**
Yen-Liang Chen, Ting-Jyun Jheng, Cheng-Zhou Zhan, An-Yeu (Andy) Wu, *National Taiwan University.*

18:20 **Low-Power Word-Parallel Nearest-Hamming-Distance Search Circuit Based on Frequency Mapping**
Hans Juergen Mattausch, Wataru Imafuku, Tania Ansari, Akio Kawabata, Tetsushi Koide, *Hiroshima University.*

THURSDAY SEPTEMBER 16

Optical Communications
(Lecture)

Session Code: C6L-H

Location: Room F

Date & Time: Thursday September 16, 2010 (17:20 - 18:40)

Chair(s): Nikos Haralabidis, *Broadcom, Greece*
Qiuting Huang, *ETH Zurich, Switzerland*

17:20 **A 5.5 Gbit/s Optical Receiver in 130 nm CMOS with Speed-Enhanced Integrated Photodiode**
Filip Tavernier, Michiel Steyaert, *KU Leuven.*

17:40 **A CMOS Adaptive Equalizer Using Low-Voltage Zero Generators Technique**
Yu-Chang Tsai, Kuo-Hsing Cheng, Yen-Hsueh Wu, *National Central University.* Ying-Fu Lin, *Faraday Technology Corporation.*

18:00 **A 10 Gb/s Adaptive Analog Decision Feedback Equalizer for Multimode Fiber Dispersion Compensation in 0.13 µM CMOS**
Mahyar Kargar, *University of California, Broadcom Corporation Irvine.* Michael Green, *University of California.*

18:20 **A 0.18-µm CMOS 1.25-Gbps Front-End Receiver for Low-Cost Short Reach Optical Communications**
Francisco Aznar, Santiago Celma, Belén Calvo, *University of Zaragoza.*

FRIDAY, SEPTEMBER 17TH, 2010

LOW POWER ELECTRONICS FOR MEDICAL APPLICATIONS IN THE FRAME OF THE FP7 ICT EUROPEAN PROJECT ULTRASPONDER.

Dr. Catherine Dehollain, *Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland*.

Summary

The two sessions in the morning are devoted to the ULTRAsponder project thanks to six presentations. They are focused on **remote powering and communications through ultrasound**, and on **low power data acquisition and low power digital processing**. The session in the afternoon is dedicated to four presentations in the domain of **low power electronics for medical applications** performed by worldwide recognized scientists.

The FP7 ICT European Project **ULTRAsponder** aims at developing a new system with a high degree of **reliability and accuracy of the clinical data**, while providing the patients with high level of safety and user friendliness. Though the project intends to propose a general solution to several possible pathologies, such as acute diabetes, epilepsy and other debilitating neurological disorders, it focuses its efforts on one **demonstrator devoted to chronic cardiac diseases**. For this specific application, **continuous monitoring** is particularly important to follow the day and night heart activity, thus allowing to understand **how the heart reacts** to different kinds of **stresses**, to different kinds of **activities** and to different sorts of **medications**. A continuous monitoring of a patient can also give the physicians the possibility to make a **direct comparison** of the actual patient condition with a past condition (one day, one week or one month earlier). Therefore continuous monitoring is a major leap forward in the diagnosis and the treatment of **cardiac congestive heart failure** (CHF).

ULTRAsponder aims at developing an innovative technology based on **ultrasonic telemetry techniques**, for communication between one sensor deeply implanted in the human body (**the transponder**) and a **control unit** which is used for both **wirelessly recharging** the implanted device and **transmitting the received information** to the external world. Web address: http://www.ultrasponder.org

Agenda
8:45: Opening of the desk at the entrance of the room

SESSION 1: **Remote powering and communications through ultrasound**

9:00: Opening of the workshop, Catherine Dehollain, EPFL, RF IC group, Lausanne, Switzerland

9:10: FP7 ICT European ULTRAsponder project: In Vivo Ultrasonic Transponder System for Biomedical applications
Speaker: Catherine Dehollain, EPFL, RF IC group, Lausanne, Switzerland

9:30: Ultrasound for wireless energy transfer and communication for implanted medical devices
Speakers: Catherine Dehollain and Francesco Mazzilli, EPFL, RF IC group, Switzerland

10:00: Possible acoustic paths for communication and energy transfer with deeply implanted sensors using ultrasound
Speaker: Benjamin Cotte, INSERM, Unit U556, Lyon, France

From **10:35 to 11.00: Coffee break**

SESSION 2: **Low power data acquisition and low power digital processing**

11:00: Data compression in medical implants
Speaker: Pal Anders Floor, Oslo University Hospital, Interventional Center, Oslo, Norway

11:35: Low-power data acquisition system for very small signals with 12-Bit-SAR-ADC
Speaker: Christof Dohmen, IMST GmbH, Kamp-Lintfort, Germany

12:10: Low power digital processing
Speaker: Marc Morgan, CSEM, Neuchatel, Switzerland

From **12:45 to 14.15: Lunch**

SESSION 3: Low power electronics for medical applications

14:15: Electro magnetical fields and implanted medical devices: MRI compatibility
Speaker: Volkert Zeijlemaker, Medtronic, Bakken Research Center, Maastricht, Netherlands

14:50: Low power analog electronics for portable and autonomous applications
Speaker: Franco Maloberti, University of Pavia, Integrated Microsystem Laboratory, Italy

15:25: RF CMOS sensors for contactless health monitoring
Speaker: Domenico Zito, University College Cork and Tyndall National Institute, Cork, Ireland

16:00: Battery-less wireless sensors based on low power UHF RFID tags
Speaker: Ivan Rebollo, Farsens S.L., San Sebastian, Spain

16:35: Closing of the workshop: Catherine Dehollain, EPFL, RF IC group, Lausanne, Switzerland

FP7 PROJECT "MULTIBASE" (SCALABLE MULTI-TASKING BASEBAND FOR MOBILE COMMUNICATIONS): ACHIEVEMENTS AND IMPACT.

Dr. Franz Dielacher, *Infineon*

FP7 project MULTI-BASE description:
In order to strengthen Europe's leading position in high-speed, end-to-end, mobile network systems technology, the MULTI-BASE consortium has identified three main areas where research will have a major impact on the advancement of state-of-the-art technology and the emergence of a sound competitive and innovative environment for the European communications and services industry:
multi-tasking radio
scalable and reconfigurable multi processor technology
algorithm/architecture co-design for maximum energy efficiency.
The MULTI-BASE project objectives target the elimination of key technical and commercial barriers to ubiquitous broadband access by enabling efficient and sustainable disposition of operation and production factors as spectrum, power engineering cost and silicon process technology.

Drawing on project research in these three areas, the MULTI-BASE consortium will demonstrate new handset baseband architectures that enable end-to-end interconnection of humans and devices, with ability to support tenfold scaling in the number of interoperating connectivity links at the same cost and power consumption as today's technology.

Agenda

09:00
Introduction to the multibase EC project
Franz Dielacher, Infineon

09:15
Trends in wireless systems and standards asking for multi-mode multi-stream radios
Liesbeth Vander Perre, IMEC

09:45
Multi-standard digital receiver frontend
Viktor Oewall, Lund-University

10:15
Multi-standard digital transmitter frontend
Wim Dehane, KU-Leuven

10:45 to 11.15 Coffee break

11:15
Reconfigurable Baseband Platform
Andreas Ehlia, Linkoeping-University

11:45–12:15
Multi-standard Algorithms
Ove Edfors, Lund-University

For further information about these workshops, please visit the webpage of the conference at http://www.esscirc2010.org/esscircWor.html

ESSCIRC FRINGE

The ESSCIRC Fringe Poster will be held in the Exhibition Area near the "Atrio III" (please refer to the map available in this program). The posters will be introduced by their authors during three different Fringe Poster Briefing Sessions on Tuesday 14th (please refer to the timetable). Poster will be then displayed from Tuesday 14th to Thursday 16th. Presenters will also be on hand to discuss their posters outside this timeslot by prior arrangement. Please come to the registration desk to arrange a discussion with any of the presenters.

P1 Low Side Switch Short Circuit Protection Optimized for High Current Inrush Loads
A. Danchiv et al., Infineon Technologies Romania, Romania

P2 Behavioral Modeling in Automotive Industry - CAN Transceiver
C. Dolea et al., Infineon Technologies Romania, Romania

P3 A 32x32 pixels vision sensor for Selective Change Driven readout strategy
P. Zuccarello et al., Universitat de Valencia, Spain

P4 A low power multi-bit phase sampling circuit for VCO based ADCs
M. Voelker, Fraunhofer Institute for Integrated Circuits, Germany

P5 Hybrid SAR-Slope ADC for CMOS Image Sensors
H. Neubauer, Fraunhofer Institute for Integrated Circuits, Germany

P6 A Radio Frequency Receiver IC for Digital Video Broadcasting - Satellite services to Handhelds
H. García-Vázquez et al., Universidad de las Palmas de Gran Canaria, Spain

P7 An Improved High-Speed High-Resolution Comparator to be Used in Pipelined Analog-to-Digital Converters
D. Yang et al., Microelectronics Technology Institute Beijing, Republic of China

P8 Pseudo H-Bridge Current Cell DAC for High Speed Continuous-Time $\Sigma\Delta$ ADCs
J. Segundo et al., University of Valladolid, Spain

P9 Low power 2.4 GHz quadrature generators for Bluetooth LE
J. Masuch et al., IMSE-CNM-CSIC and University of Seville, Spain

P10 A Parallel Continuous-Time $\Sigma\Delta$ ADC for OFDM UWB Receivers in 130 nm CMOS Technology
J. Segundo et al., University of Valladolid, Spain

P11 Design of Injection-Locked Frequency Divider in 65 nm CMOS Technology for mm-W applications
D. Brandano et al., UPC, Spain

P12 Analog Circuit Synthesis: EDA'S Nightmare and Designer's Dream
A. Momin, TES Electronic Solutions GmbH, Germany

P13 Sensitivity Analysis Based Analytical Evaluation of Aging Degradation in Linear Circuits
S. More et al., Technische Universität München, Germany

P14 A Low-voltage Current-mode Log-domain Integrator using MOS in Sub-threshold
L. Ramezani, Islamic Azad University, Iran

P15 Synaptic Weight Storage and Update In Silicon Neurons
A. Smith, University of Liverpool, UK

P16 A Signal Processing System for Recognition of Acoustic Emergency Signals
M. Mielke, University of Siegen, Germany

P17 12.5 Gbit/s Configurable Threefold 2:1 MUX and 1:2 DEMUX Chips in 130 nm CMOS Technology
H. Huang et al., University of Stuttgart, Germany

P18 Dual-Mode Switched-Capacitor DC-DC Converter for Subthreshold Processors with Deep Sleep Mode
J. De Vos et al., Université Catholique de Louvain, Belgium

P19 In-Situ Monitoring to Adapt for PVT-Variations
M. Wirnshofer et al., Technische Universitat Munchen, Germany

P20 S-Parameter Measurement-Based Modeling Methodology for On-Chip Interconnects used in High Frequency Systems
O. González-Díaz et at., INAOE, Mexico

P21 A FPP-Oriented Tone Mapping Technique for High Dynamic Range Imagers using Temporal and Final Exposure Measurements
S. Vargas-Sierra et al., IMSE-CNM-CSIC and University of Seville, Spain

NOTES